

## VOLTAGE TO FREQUENCY CONVERTER

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**Abstract** – Voltage to frequency converter (VFC) is an oscillator whose frequency is linearly proportional to control voltage. The charge balanced VFC may be made in asynchronous or synchronous (clocked) forms. The synchronous charge balanced VFC or "sigma delta" ( $\Sigma$ - $\Delta$ ) VFC (SVFC) is used when output pulses are synchronized to a clock. The charge balance VFC is more complex, more demanding in its supply voltage and current requirements, and more accurate. It is capable 16 to 18 bit linearity. The synchronous behaviour is good in many applications, but the output of SVFC is not a pure tone (plus harmonics) like a conventional VFC, but it contains components harmonically related to the clock frequency.

In this paper, the new SVFC (NSVFC) is described. This NSVFC works similarly as conventional SVFC but it has a pure tone on output (for constant input voltage). Therefore, it is possible to measure the period of NSVFC output (this does not possible for SVFC).

Keywords: A/D converters, voltage to frequency converter, sigma delta modulator.

### 1. INTRODUCTION

In recent years, VFC have become quite popular due to their low cost and application versatility in variety of electronic control and measurement systems. With a good quality VFC, this circuit will match the performance of many commercial A/D converters. Its only disadvantage is relatively slow conversion time.  $\Sigma$ - $\Delta$  modulator [1] can be used for synchronous VFC (SVFC). In SVFC charge balance pulse length is now defined by two successive edges of the external clock. If this clock has low jitter the charge will be defined very accurately. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and they have excellent temperature stability [2], but is not pure tone for constant input voltage. The block diagram of the  $\Sigma$ - $\Delta$  VFC is shown on Fig. 1. Fig. 2 shows the waveforms of  $\Sigma$ - $\Delta$  SVFC. From Fig. 2 can be seen, that output periods are not the same, but they have changed between 3 and 4 clock cycles. This disadvantage was taken away in NSVFC.

### 2. NEW SYNCHRONOUS VFC

In Fig. 3 is NSVFC block diagram. Only one-shot is added and connected to comparator output. Fig. 4 shows

waveforms of this NSVFC. Number of pulses is same for usual  $\Sigma$ - $\Delta$  SVFC and NSVFC, but for NSVFC the frequency is linearly proportional to a control voltage (input voltage must be offset in converter [2]).

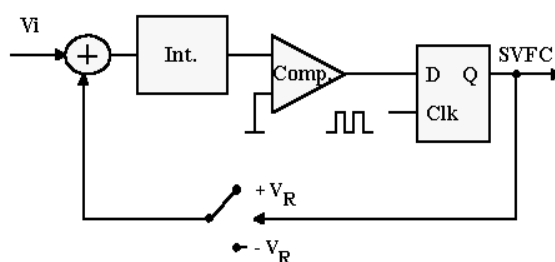


Fig. 1.  $\Sigma$ - $\Delta$  voltage to frequency converter. Int. - integrator, Comp. - comparator,  $V_i$  - input voltage,  $V_R$  - reference voltage, D - flip flop

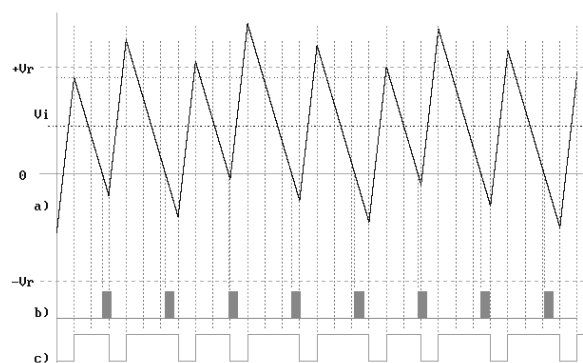


Fig. 2. Waveforms of  $\Sigma$ - $\Delta$  SVFC. a) integrator output, b) comparator output, input voltage  $V_i = 1.8$  V, reference voltage  $V_R = 4$  V.

The output frequency  $f_O$  is given by (1):

$$f_O = f_{CLK} (1 - V_i / V_R) / 2 \quad [\text{Hz, V}] \quad (1)$$

where  $V_i$  is input voltage,  $V_R$  is reference voltage and  $f_{CLK}$  is clock frequency.

If  $V_i = V_R - V_{ii}$ , then

$$f_O = 0,5 f_{CLK} (V_{ii} / V_R) \quad [\text{Hz, V}] \quad (2)$$

where  $V_{ii}$  is input voltage with offset.

### 3. NSVFC OUTPUT FREQUENCY EVALUATION

The key to  $\Sigma$ - $\Delta$  modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the

integrator is feed to 1-bit analog/digital converter (ADC). This is simply a comparator with its reference input at a level of half the input range, 0 V in this case. The ADC output feeds a 1-bit digital/analog converter (DAC) which has output levels equal  $+V_R$  or  $-V_R$ . A summing amplifier completes the loop by summing the current input signal and

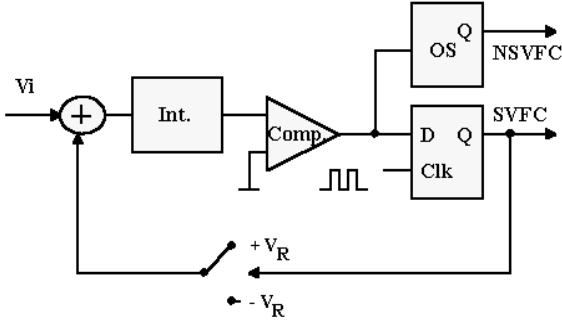


Fig. 3. New  $\Sigma$ - $\Delta$  voltage to frequency converter. Int. - integrator, Comp. - comparator,  $V_i$  - input voltage,  $V_R$  - reference voltage, D - flip flop, OS - one shot.

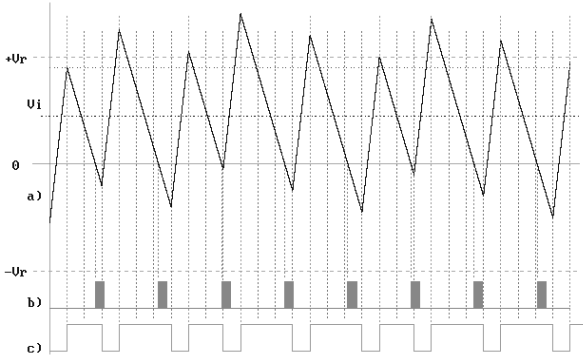


Fig. 4. Waveforms of NSVFC. a) integrator output, b) one shot output, c) D-flip flop output.  $V_i = 1,8$  V,  $V_R = 4$  V, period of one shot is  $3,636 T_{clk}$

the previous sample DAC output. The aim of the feedback loop is to try to maintain the average output of the integrator at the comparator reference level, 0 V. Therefore:

$$\sum_{k=1}^{\infty} V_{o1}(k) + \sum_{k=1}^{\infty} V_{o2}(k) = 0 \quad (3)$$

where  $k = 1, 2, \dots, \infty$ , and  $V_{o1}(k)$  and  $V_{o2}(k)$  are integrator output voltage in  $k$  output frequency period, see Fig. 5. Change  $\Delta V_a$  is given by (4):

$$\Delta V_a = C \int_0^{T_{clk}} (V_i(t) + V_R) dt \quad (4)$$

and  $\Delta V_b$  is given by (5):

$$\Delta V_b = C \int_0^{nT_{clk}} (V_i(t) - V_R) dt \quad (5)$$

where  $C$  is the integrator constant. The integrator output is given by:

$$V_{o1}(k) = V_{o2}(k-1) + C \int_0^{T_{clk}} (V_i(t) + V_R) dt \quad (6)$$

$$V_{o2}(k) = V_{o1}(k) + C \int_{T_{clk}}^{(n+1)T_{clk}} (V_i(t) - V_R) dt \quad (7)$$

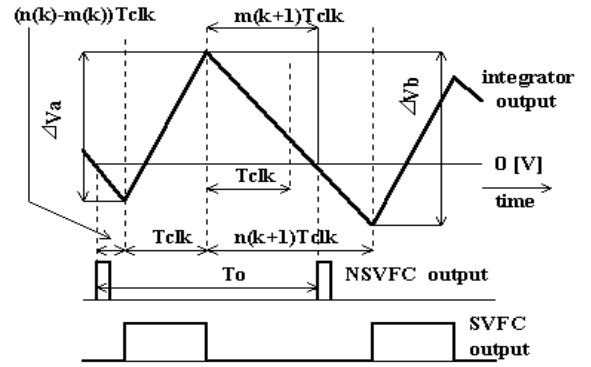


Fig. 5. Detailed waveforms of the integrator, D flip-flop SVFC and one shot NSVFC outputs,  $n=2$  in this Fig. ( $nT_{clk} = 2T_{clk}$ ).

and for  $V_i(t) = V_i$ :

$$V_{o1}(k) = V_{o2}(k-1) + C(V_i + V_R)T_{clk} \quad (8)$$

$$V_{o2}(k) = V_{o1}(k-1) + C(V_i - V_R)nT_{clk} \quad (9)$$

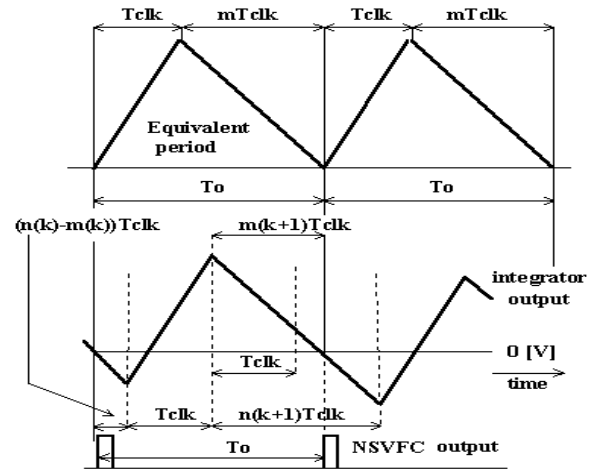


Fig. 6. NSVFC waveforms and equivalent time diagram for period derivation

Integrator output voltage change is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)nT_{clk} \quad (10)$$

where  $n$  must be an integer for SVFC. For NSVFC output is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)mT_{clk} \quad (11)$$

where  $m$  is real for NSVFC. From (11) ( $V_R > V_i$ ):

$$m = \frac{V_i + V_R}{V_R - V_i} \quad (12)$$

for SVFC,  $n$  is given by (13):

$$n = \text{ceil} \left( \frac{V_i + V_R}{V_R - V_i} \right) = \text{ceil}(m) \quad (13)$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9,01/3)=4.

Output period for NSVFC is given by (14):

$$T_o = T_{clk} [n(k)-m(k)+1+m(k+1)] \quad (14)$$

but this equation is not good for output period expression. Output period for NSVFC can be determined from equivalent period waveform from Fig. 6:

$$T_o = T_{clk} (1+m) \quad (15)$$

where  $m$  is given by (12) for constant  $V_i$  and NSVFC output frequency is:

$$f_o = 1/T_o = f_{clk} (V_R - V_i)/2V_R \quad (16)$$

From (16) is shown, that NSVFC output frequency is linearly dependent on input voltage ( $f_{clk}$  and  $V_R$  are constants).

#### 4. EXPERIMENTAL RESULTS

SVFC AD7741 and AD7742 [2] were tested and NSVFC was simulated and realized.

Table 1. Some measured values  $V_i$  and  $f_o$  of realized experimental NSVF

$V_i$	0,00	0,10	0,50	1,01	1,20	V
$f_o$	3,57	3,53	3,28	3,03	2,93	kHz

$V_i$	1,41	1,61	2,01	2,51	3,01	V
$f_o$	2,84	2,73	2,53	2,28	2,02	kHz

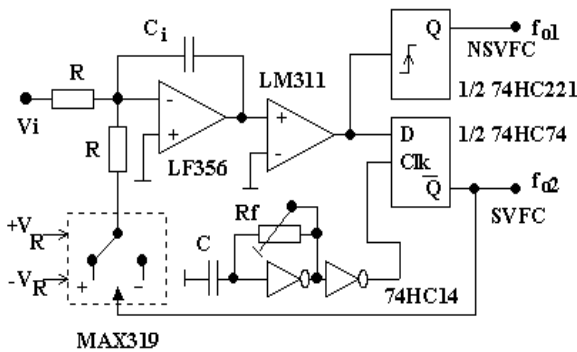


Fig. 7. Experimental NSVFC simplified circuit diagram.

Simulation was performed at the block diagram level of Fig. 3. The simulation program was also developed. The NSVFC was realized and simulation results and measured results were compared. In Fig. 7, experimental realized NSVFC is shown [3]. In Fig. 8, graph of measured voltage/frequency characteristic of experimental NSVFC is shown. In Tab. 1, some measured values  $V_i$  and  $f_o$  are displayed.

In Fig. 9, the oscilloscope photograph shows the integrator output and D-flip flop output of SVFC. In Fig. 10, the oscilloscope photograph shows also integrator output and one shot output of NSVFC.

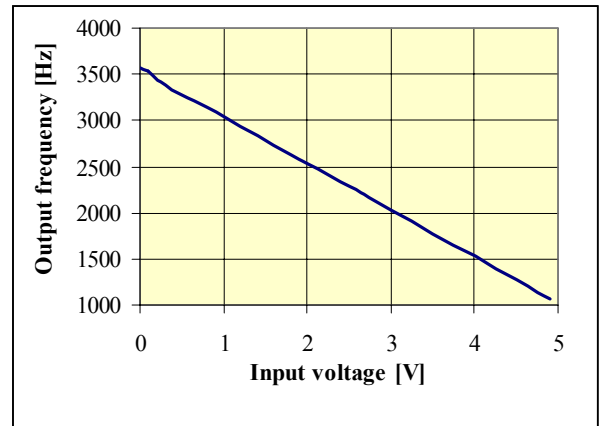


Fig. 8. Graph of voltage/frequency characteristic of realized experimental NSVFC

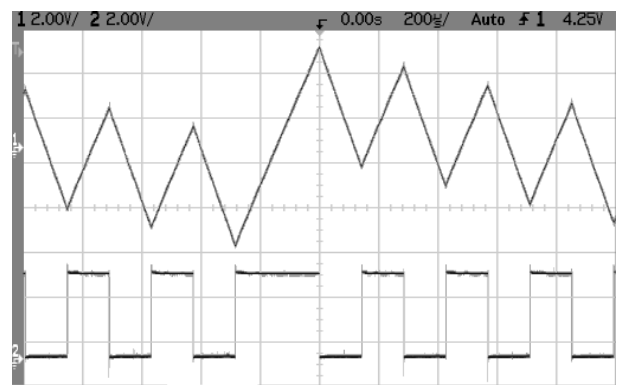


Fig. 9. The oscilloscope photograph of the integrator and D-flip flop output of SVFC.

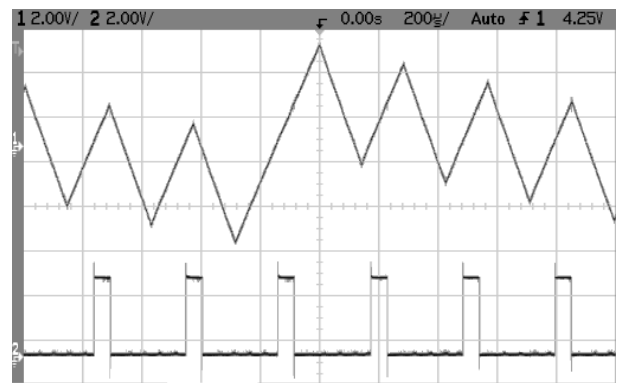


Fig.10. The oscilloscope photograph of the integrator and one shot output of NSVFC.

#### 5. CONCLUSION

Analysis, simulation and prototype of new type voltage to frequency converter were described in this paper. It was pointed out that this new converter has better properties than other synchronous types of VFC.

In common type of SVFC, since the output pulses are synchronized to a clock they are not equally spaced (Fig. 9). This need not affect the user of a SVFC for A/D conversion, but it does prevent its use as a precision oscillator. Despite this disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC

applications. This main disadvantage of SVFC described above was removed in new type of NSVFC (See Fig. 10).

In Fig. 11, the frequency spectrum of SVFC is shown and in Fig. 12, the spectrum of NSVFC is displayed. From Fig. 12 can be seen, that spurious spectral lines are rejected.

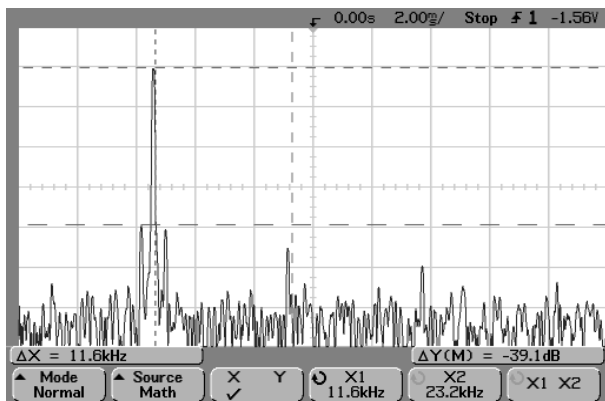


Fig. 11. The frequency spectrum of traditional  $\Sigma$ - $\Delta$  V/f converter.

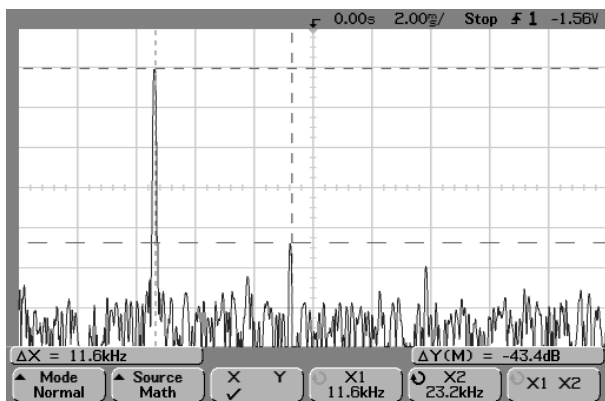


Fig. 12. The frequency spectrum of new, modified  $\Sigma$ - $\Delta$  V/f converter (NSVFC).

Because output pulses are equally spaced in NSVFC, this device can be used as fractional divider in fractional phase locked loop.

## ACKNOWLEDGMENT

This research work has been supported by New Technologies - Research Centre in West Bohemian Region LN00 B084 and partly also by Spezial-Electronic (Maxim IC's).

## 6. REFERENCES

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