Increasing of Sampling Rate of Internal ADC in Microcontrollers by Equivalent-Time Sampling

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***Abstract* – The paper describes the Equivalent-Time Sampling (ETS) in Software-Defined Instruments (SDI) - typically oscilloscopes. It introduces a possible solution of the microcontrollers drawback caused by the maximal sampling frequency and its limitations in digitizing quick transient responses. The principle of ETS used in microcontrollers is explained, and the jitter effect is taken into account. Analog-to-digital converter input model and real properties of software-defined oscilloscope from ETS point of view are introduced and explained. In the system for circuit behavior analysis as a step response, where a microcontroller with internal peripherals (pulse-width modulation and analog-to-digital converter) is used for a test signal generation and data digitization, the use of ETS may increase the equivalent sampling rate of the internal analog-to-digital converter up to tens of MSa/s.**

I. INTRODUCTION

Most current microcontrollers (MCU) are equipped with internal analog-to-digital converters (ADC). The used type of ADC is usually the Successive Approximation Register (SAR) architecture [1]. MCU with SAR ADC is very often used in measuring applications, where they are used for digitization of DC or quasi-static voltages. Another area is the digitization of AC voltages, e.g., measurement in the power line, power measurement, effective values of voltage and current measurement, or motor control where the digitization of controlling signals may require the sampling with a sufficiently high frequency. Notwithstanding, in signal digitization, the sampling frequency is chosen to fulfill the sampling theorem ($f_s > 2 \cdot f_m$, where f_s is the sampling frequency, and f_m is the maximal frequency of the sampled signal). This sampling is referred to as Real-Time Sampling (RTS).

Thanks to the growing power of MCUs, which are also equipped with a number of peripherals to process analog signals (ADC, Operational Amplifier, Analog Comparators, Digital-to-Analogue Converter - DAC), it is possible to use them for software-defined instruments (SDI) [2]. All instrument functions are implemented only by programming and using the internal peripherals of the microcontroller without the need for external circuits. This was the situation at Czech Technical University in Prague (CTU), Faculty of Electrical Engineering (FEE), Department of Measurement, where several SDIs were developed and are used as a replacement for standard measuring instruments (typically digital oscilloscopes) in individual projects or as part of a Home Lab in distance learning [2] – [3]. However, the limitation of such an SDI is given by the maximal sampling frequency, which, in the case of internal ADCs in microcontrollers, is commonly from hundreds of kSa/s to a maximum of few units MSa/s. The corresponding bandwidth of an oscilloscope implemented by SDI is tens to hundreds of kHz. Thus, the measurement tasks are limited. For example, measurement of frequency characteristics of the circuit, determination of the circuit bandwidth – a cut-off frequency etc. If the SDI includes a functional signal generator, an internal DAC connected to the internal output buffer is used. This combination makes it possible to generate harmonic signal approximations, but typically, at frequencies up to tens of kHz, which is insufficient to evaluate the system's behavior (amplifiers, operational amplifiers - OA, etc.) on a broader scale frequency range. System response to a unit step function also describes the system's dynamic behavior in the tasks such as determining the time constant of a system, a slew rate of the OA, etc. Even in simple SDIs, there is a periodic pulse signal PWM, which has sufficiently steep edges. The classical method of determining the system response would be using a real-time oscilloscope with a sufficiently high sampling rate f_s. However, in the case of SDI, the limitation is given by the conversion time of the internal ADC. Therefore, it is necessary to find another way to solve the limitation. This article presents the solution using the Equivalent-Time Sampling (ETS) principle, which may increase the equivalent sampling rate of the internal analog-to-digital converter of the microcontroller up to tens of MSa/s.

II. EQUIVALENT-TIME SAMPLING IN MCU

The ETS principle is used for digitizing the periodic signal in many areas, for example, in oscilloscopes or radio applications [4] – [10]. In SDI oscilloscopes, the simplest form of ETS is used at the Department of Measurement. The idea is that the periodic signal is digitized at a precisely defined speed to the fundamental frequency. The only requirement of ETS is that the analog input bandwidth of the ADC is sufficient and does not limit the spectrum of the digitized signal. ETS used in the internal ADC of the MCU can be implemented as stroboscopic sampling. The digitized signal is strictly periodic with the fundamental frequency f_{PWM}, and its digitization takes place at a speed of f_{SAMP} very close to the f_{PWM}. Only one sample is taken in each period. This results in aliasing.

The ETS model can also be implemented by skipping one or more signal periods and taking a sample after k_s periods (where k is an integer). Thanks to this, it is possible to digitize a signal whose frequency is significantly higher than the f_{SAMP}. However, a sufficient analog input bandwidth of the ADC is necessary for this ETS mode.

To verify the analog input bandwidth of the internal ADCs in the MCUs, experiments were performed according to the connection in Fig. 1 [11].

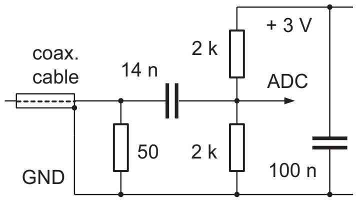

Fig. 1. Connection for ADC bandwidth verification.

The HP 8647A harmonic signal generator is connected to the ADC input via a set of capacitors connected in parallel. The resistance divider sets the DC signal offset to a level suitable for ADC input. The generated signal was digitized with an internal ADC with f_{SAMP} in order of hundreds of kSa/s. The generated frequencies were chosen very close to a multiple ADC f_{SAMP} to obtain the aliased signal with a sufficiently high number of samples per period. STM32 series MCU was used for the measurements (F051, F303, F407), each of them with slightly different internal ADC.

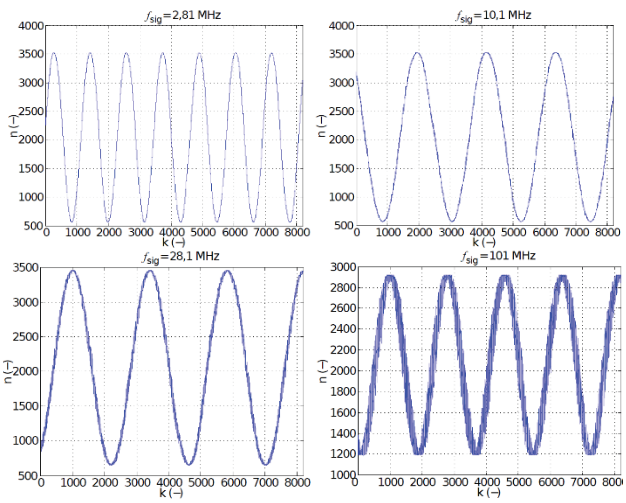

Fig. 2. Signals digitized by the F303s ADC

The analog input bandwidth of the ADC could be estimated from the decrease in the amplitude of the aliased signal. An example of the signal digitized by the ADC in F303 is shown in Fig. 2.

With the increasing frequency of the signal, the jitter caused by a random relative shift of the generated harmonic signal f_{SIG} and the f_{SAMP} becomes more and more apparent. At high signal frequencies, the effect of the input signal crosstalk via parasitic capacitances to the SAR ADC block could also occur and affect the SAR process by the charge transfer. The MCU internal ADCs analog input bandwidth characteristics are shown in Fig. 3.

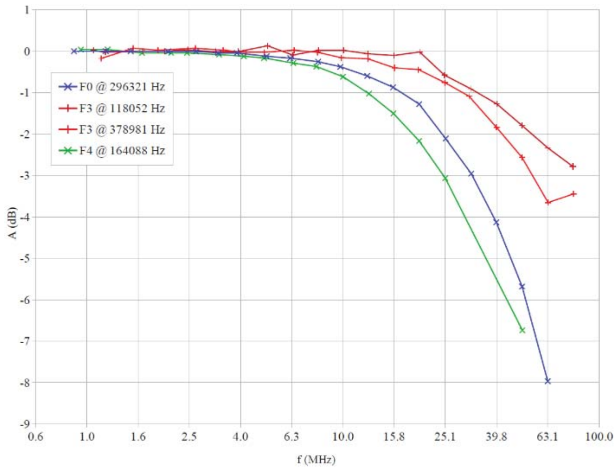

Fig. 3. Frequency characteristics of internal ADC inputs of selected MCU

The characteristics show that all tested MCUs have an ADC analog input bandwidth in the order of tens MHz, sufficient for laboratory teaching experiments with SDI oscilloscopes operating in ETS mode.

Effect of Jitter at ETS

As mentioned above, the presented method assumes a strictly periodic input signal with a constant frequency. Any changes in frequency or random shifts in sampling acquiring times cause a degradation of the aliased signal [12]. This is also evident from the measurement presented in Fig. 2. At higher input signal frequencies, the resulting digitized signal appears to be noisy in the presented records, which, however, is caused by jitter [13] or [14]. To determine the jitter, further measurements were performed with the STM32F303VC [11]. The detail of the measured signal at the f_{SIG} = 217.7062 MHz is in Fig. 4.

Inspecting the record in the range k = 0 to 600, it can be seen that the minima approximately follow the value n = 1800. In addition, the local changes in the n position between samples in this area are lower. Thus, it can be stated that this is primarily the effect of jitter. To estimate the jitter, two adjacent samples in the part of the digitized signal with the high steepness were selected; k = 1081 and corresponding n = 2191 and following k = 1082 and corresponding n = 1884, which have the largest difference in the value of n. To determine the size of the jitter, the corresponding points on the idealized sinewave signal are found to have the same n value. These were the positions corresponding to α_1 = -0.68 rad and α_2 = 0.55 rad. This is a phase difference $\Delta\alpha$ = 1.23 rad, that is 0.195 periods, which at 217.7 MHz represents a time of 0.9 ns. The same analysis was performed for a frequency f_{SIG} = 101 MHz when the detected jitter value was 0.86 ns.

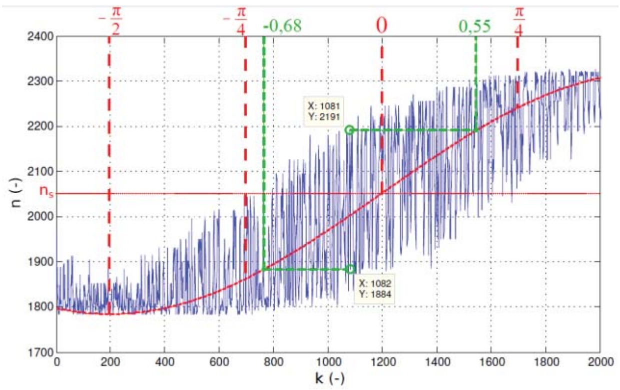

Fig. 4. The detail of the measured signal

The measurement results indicate high requirements for the precise relative sampling timing for the input signal during stroboscopic sampling.

In the case of MCU that use PWM, which frequency is derived from a stable generator of the system clock with frequency f_{SYS} and the sampling times are derived from timers and f_{SYS}, this requirement may be met. The situation is different for simpler MCUs such as the ATmega 328, part of the widely used Arduino module. In this case, the sampling times of ADC are not controlled by a timer but by software, which raises problems with accurate timing.

III. USE OF ETS IN SDI IMPLEMENTED BY MCU

Simple SDI oscilloscopes implemented with STM32F042 or STM32G030 and used as a Home Lab have a maximum sampling rate of 500 kSa/s. If it is necessary to evaluate the response of faster circuits, stroboscopic sampling, which is the ETS method, can be used to increase the sampling rate. The PWM signal generated by the respective peripheral is used to excite the tested circuit. Usually, where it is only necessary to determine the circuit's response to a unit step function signal, the frequency of the PWM signal in the order of units of kHz and the corresponding T_{PWM} period in the order of tens of ms are used. The output signal of the tested circuit is sampled in a way that only one sample is taken in each of its periods. The sampling period T_{SAMP} is chosen to be very close but slightly larger than the PWM signal period T_{PWM}. As a result, the sampling time shifts by ΔT relative to the PWM signal by every sample. If the T_{PWM} and the T_{SAMP} were the same, then ΔT = 0, and a sample would be taken approx. The same signal position. This principle can be used to check the stability of the T_{SAMP}.

If $T_{PWM} < T_{SAMP}$ applies, then the moment of signal sampling at each equivalent time period shifts relative to the PWM signal by a time T_{SEQ}.

$$\Delta T = T_{SAMP} - T_{PWM} = T_{SEQ} \qquad T_{PWM} \le T_{SAMP} \tag{1}$$

There are several samples per T_{PWM}, which corresponds to the situation as the PWM signal was sampled with a T_{SEQ}, (2) and corresponding $f_{SEQ} = 1/T_{SEQ}$.

$$T_{SEQ} = T_{SAMP} - T_{PWM} = \frac{1}{f_{SAMP}} - \frac{1}{f_{PWM}} = \frac{f_{PWM} - f_{SAMP}}{f_{PWM}} \cdot T_{SAMP} \tag{2}$$

The situation is shown in Fig. 5, where S_{IN} is the input signal of the ADC, S_{DIG} represents the digitized signal in real-time, and S_{RECON} is the reconstructed signal by ETS.

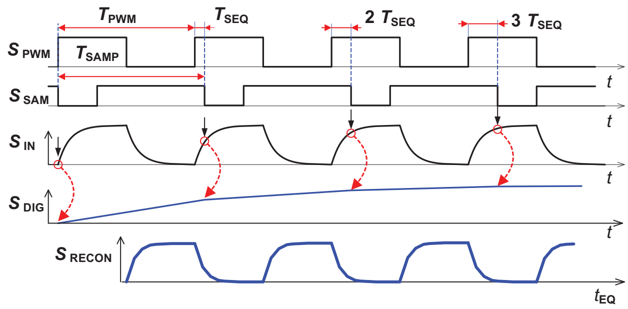

Fig. 5. Signal digitization timing in ETS

If the frequency difference Δf is positive, the f_{SEQ} will also be positive, and the relative sampling points in the time will be shifted to the right in a positive time.

$$f_{SEQ} = \frac{f_{PWM}}{f_{PWM} - f_{SAMP}} \cdot f_{SAMP} = \frac{f_{PWM}}{\Delta f} \cdot f_{SAMP} \\ \Delta f = f_{PWM} - f_{SAMP} \tag{3}$$

However, if Δf is negative, the f_{SEQ} will also be negative, and the sampling points will shift to the left on the equivalent time axis. The obtained reconstructed signal will be mirrored. It also follows from (3), the smaller the difference Δf, the more significant the increase in the equivalent sampling frequency. Thus, an acceleration coefficient of equivalent sampling can be defined as $k_{AEQ} = f_{PWM}/\Delta f$.

The situation where only one sample is taken per PWM signal period is suitable for equivalent sampling. It is necessary to have a detailed record of the response to the input change - typically a unit step function.

However, sometimes it is useful to use equivalent sampling to inspect the circuit's response to a periodic signal with a higher frequency than the sampling frequency. In this case, the situation changes slightly compared to the situation described above. The sample will be taken only once per k_s period, where k_s is a natural number. The equivalent sampling frequency will be defined by (4)

$$f_{SEQ} = \frac{f_{PWM}}{f_{PWM} - k_S \cdot f_{SAMP}} \cdot f_{SAMP} \qquad k_S \approx \frac{f_{PWM}}{f_{SAMP}} \tag{4}$$

The acceleration coefficient k_{AEQ} of the equivalent sampling frequency compared to the real sampling frequency f_{SAMP} is according to (5)

$$k_{AEQ} = \frac{f_{PWM}}{f_{PWM} - k_S \cdot f_{SAMP}} \tag{5}$$

In MCUs, all periodic events are usually derived from the system clock f_{SYS}. The f_{SAMP} and f_{PWM} are also derived by dividing by the coefficient M and N, respectively, using timers.

$$f_{SAMP} = \frac{f_{SYS}}{M} \qquad f_{PWM} = \frac{f_{SYS}}{N} \tag{6}$$

Then, f_{SEQ} is defined by

$$f_{SEQ} = \frac{f_{PWM}}{f_{PWM} - k_S \cdot f_{SAMP}} \cdot f_{SAMP} = \frac{f_{SYS}}{\mathrm{N}} \cdot \frac{1}{\frac{f_{SYS}}{\mathrm{N}} - k_S \cdot \frac{f_{SYS}}{\mathrm{M}}} \cdot \frac{f_{SYS}}{\mathrm{M}} \tag{7}$$

And after simplification

$$f_{SEQ} = \frac{f_{SYS}}{M - k_S \cdot N} \tag{8}$$

It follows from (8), the maximum ETS frequency in the MCU can be $f_{SEQ} = f_{SYS}$ for $M - k_sN = 1$. Theoretically, the ETS frequencies in the MCU can take be values where n in (8) is a natural number (1, 2 …).

$$f_{SEQ} = \frac{f_{SYS}}{n} \tag{9}$$

For example, in an oscilloscope with ETS by a MCU STM32G03J6 with f_{sys} = 64 MHz, ETS frequencies can be used f_{SEQ} = 64.0; 32,0; 21,3; 16.0; 12,8; 8,0; … MSa/s.

If the $M - k_sN = 0$, then f_{SEQ} would equal infinity, and the PWM signal would still be sampled in one spot. If the $M - k_sN$ will be negative (-1, -2 …), f_{SEQ} will also be negative, and the signal will be mirrored, but this may not be a problem for some experiments.

When using SDI with an MCU in the form of an oscilloscope, there are tasks such as inspecting the circuit's response to signals with different frequencies. A standard measurement would use a harmonic signal, which is impossible when using a PWM MCU. However, evaluating the system's behavior in response to rectangular signals at different frequencies can provide the necessary information.

IV. ADC INPUT MODEL AND PROPERTIES OF SDI SCOPE FROM ETS POINT OF VIEW

A typical MCU often contains only one ADC to whose inputs the signal can be fed from different input pins using a multiplexer. The simplified equivalent scheme in Fig. 6. Circuit on the left assumes one input channel selected by the multiplexer contains only the basic parts and does not include other parasitic capacitances.

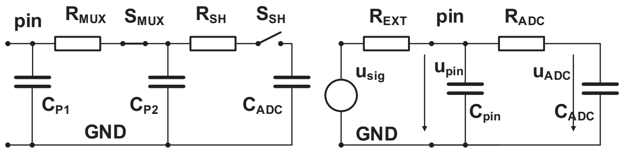

Fig. 6. ADC input equivalent scheme(left) and according to catalog data (right)

There are at least two switches in the signal path. The first is implemented by a multiplexer S_{MUX}; the second is by a switch S_{SH} of the sampling circuit. Each of them can be represented by a resistance R_{MUX} and R_{SH}. The size of the parasitic capacitances is also crucial for evaluating dynamic behavior, where CP1 represents the parasitic capacitance of the pin, CP2 corresponds to the internal parasitic capacitances of the multiplexer C_{ADC} represents the capacity of the SAR ADC itself. For the estimation of the ADC input behavior, the parameters C_{ADC} = 5 pF, C_{P1} = 8 pF and C_{P2} = 2 pF, R_{MUX} = 250 Ω, R_{SH} = 250 Ω for F303 and C_{ADC} = 8 pF, C_{P1} = 8 pF and C_{P2} = 2 pF, R_{MUX} = 300 Ω, R_{SH} = 300 Ω for F051, were used for the model according to Fig. 5. Performed simulations confirmed the results presented in Fig. 3.

In the catalog of MCUs, the parameters can be found corresponding to the model in Fig. 5 (right), where the ADC input is excited by an external signal source u_{sing} an internal resistance R_{EXT}. R_{ADC} includes resistances R_{MUX} and R_{SH}. For F051 MCU, the ADC input equivalent scheme parameters are given as C_{ADC} = 8 pF and R_{ADC} = 1 kΩ. The minimum bandwidth of the ADC input is determined as

$$f_B = \frac{1}{2 \cdot \pi \cdot R_{ADC} \cdot C_{ADC}} = \frac{1}{2 \cdot \pi \cdot 1000 \cdot 8 \cdot 10^{-12}} = 20\ \mathrm{MHz} \tag{10}$$

The analog bandwidth of the ADC input, according to Fig. 3, is valid only for the small R_{EXT} of the signal source, which will be negligible to R_{ADC}. With large R_{EXT} values, a very simplified equivalent model corresponding to the RC circuit according to Fig. 7 can be used.

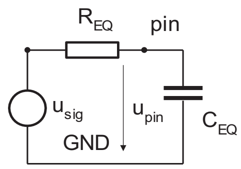

Fig. 7. ADC input scheme for a large value of R_{EXT}

Where the C_{EQ} includes C_{ADC} and other parasitic capacitances, the R_{EQ} resistor includes R_{EXT} and R_{ADC}.

The ADC behaves differently in the ETS mode in terms of sampling. The sampling time when the S_{SH} is switched on can be significantly longer than the period of the digitized signal. It can be a track and hold mode. The moment of sampling is determined by the moment of opening the S_{SH}. At the tracking time, the measured circuit is loaded with the total capacity determined as the

$C_{P1} + C_{P2} + C_{ADC}$. In the end, the S_{SH} opens, and the C_{ADC} is disconnected from the circuit. During the subsequent AD conversion in the ADC with charge redistribution, the voltage u_{ADC} changes to the default value, which can be marked as the residual voltage U_{RES}.

Even if the constant voltage U_{IN} is sampled repeatedly, the measured circuit must supply a charge (positive or negative) to the ADC input, which magnitude depends on the $\Delta U = U_{IN} - U_{RES}$. This causes a transient at the input, causing a short-term change (negative or even positive) of the u_{PIN}. The advantage of ETS over Real-Time Sampling (RTS) is that even a large sampling time value can be used when the ADC is in track mode, that the transient can finish in advance before the actual u_{ADC} value is sampled.

V. PRACTICAL REALIZATION OF SDI WITH ETS

The ETS method has been successfully used in SDI oscilloscopes with various STM32 MCUs (developed software is available at *https://leo.fel.cvut.cz/*). These were either ready-made modules Nucleo, Blue Pill or Black Pill, or standalone MCUs on developed PCB adaptor. Only modules or MCUs without any specialized accessories were used in all cases. This allows SDI to be implemented only by uploading the firmware and running a PC application. In the RTS, maximum sampling rates are in the order of hundreds of kSa/s to a few units MSa/s, but if the ETS is used, the limitation is given practically only by the f_{SYS} according to (9).

The experiment with the SDI [3] based on STM32G030J6M3 MCU has been performed. The sampling rate in RTS is only 3x 200 kSa/s (T_{SAMP} = 5 µs), but using ETS, it is extended to 1x 64 MSa/s (T_{SEQ} = 0.0156 µs), which is presented as an application example of the described method. The experiment aims to demonstrate the effectiveness of ETS by determining the slew rate of the MCP601 OA as a step response. Fig. 8 shows an experiment with the SDI implemented in MCU and the tested MCP601 OA.

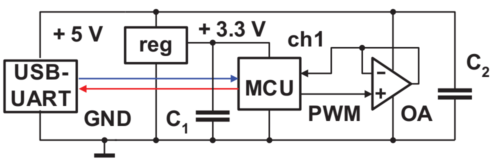

Fig. 8. Experiment connection

The parameters of the experiments are; f_{PWM} = 10 kHz, f_{SAMP} = 9998,437 Hz, f_{SEQ} = 64 MSa/s, k_{AEQ} = 6401. Fig. 9 shows measured step response of the OA.

The measured interval 6.403 ms corresponds to an equivalent time of 1 µs, and the slew rate of the tested OA is measured to SR = 2.2 V/µs, which roughly corresponds to the catalog data of 2.3 V/µs. The same OA has been measured by the HP54622D oscilloscope (RTS = 200 MSa/s), and the measured SR = 2.18 V/µs confirmed the accuracy of the SDI. Looking at Fig. 9, it is clear that in RTS, where T_{SAMP} = 5 µs, the slew rate of approx. Two µs ends faster, and no information would be obtained. However, thanks to ETS with T_{SEQ} = 0.0156 µs, the time resolution for determining the SR is sufficient.

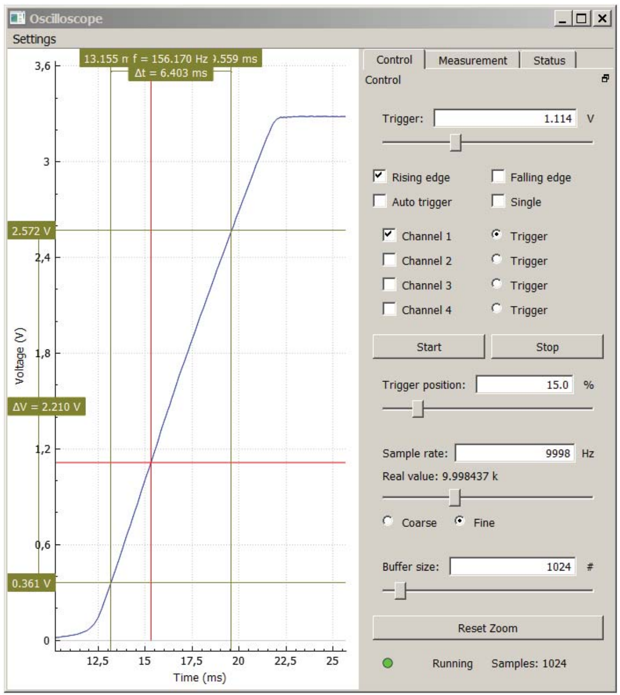

Fig. 9. The measured step response of MCP601

This experiment confirmed the applicability of even very simple SDI oscilloscopes for similar dynamic measurements.

VI. CONCLUSION

The paper presented the principle of equivalent time sampling, where the microcontroller's internal peripheries are used for test signal generation and data digitization. The ETS method has proven very useful in simple oscilloscope-type devices implemented using microcontrollers. ETS, an equivalent sampling rate can be increased up to 100 MSa/s and can be used, for example, for inspecting the step response of the circuit.

During the experiments, the focus was on selected types of MCUs of the STM32 series, which were used at the CTU, FEE, Department of the Measurement as SDI in standard, and distance teaching as the Home Lab. The described principle of ETS and the method of implementation of SDI can be successfully used in the broader range of microcontrollers, such as Arduino. They can find use in other areas of measurement.

VII. ACKNOWLEDGMENTS

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