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Measurement issues on harmonic analysis according to the IEC 61000-4-7

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***Abstract* – The objective of this article is an analysis of measurement issues related to the implementation of digital signal processing techniques for harmonic analysis, by means of FFT algorithm with different interpolation algorithms (linear, quadratic and cubic) and different sampling rates. A comparative analysis is made on errors on harmonics measurement obtained in the various case study analyses. Such errors are compared with the IEC 61000-4-7 limits. The study is supported by both simulation and experimental tests; these last are performed with different acquisition boards for signals acquisition.**

Keywords: harmonic analysis, power quality, power system measurements, IEC 61000-4-7

I. INTRODUCTION

Harmonics measurement of voltage or current is one of the key elements in the framework of power quality (PQ) assessment in power systems and there is an increasing interest in the integration of such measurements in common smart metering platforms. Several techniques can be found in literature for the implementation of spectral analysis for PQ measurements [1]–[4].

One of the most known algorithms is the Discrete Fourier Transform (DFT), which is also the one mainly considered by the IEC 61000-4-7 Standard. This algorithm can be used to estimate the amplitude of the harmonic components of the signal whatever the number of acquired samples available (not necessarily a power of two); this can be useful when the number of samples must be chosen to obtain a given observation window (for example 200 ms according to IEC 61000-4-7), depending on the sampling frequency of the data acquisition device. On the other hand, the main disadvantage of DFT is the computational cost, which is $O(N^2)$, being N the number of samples; in fact, if the measurement need is to obtain the spectral analysis results in a short time, it is necessary to have high-performance hardware. An alternative to DFT is its faster version, i.e. the Fast Fourier Transform (FFT) [5]–[8]. This algorithm has a computational cost lower than the DFT one, being equal to $Nlog_2(N)$; however, it needs N to be equal to a power of 2, to obtain the best computational performance.

This may pose a constraint in terms of sampling frequency, which should be set in accordance with the signal frequency and in order to allow having a proper number of samples for the FFT (in the specified synchronous observation window specified by the IEC Standards [1]-[2]). When this is not possible (for example in already existing devices with fixed or few selectable values for sampling frequency), a possible solution can be to use interpolation or zero padding techniques. In both cases they will cause some approximation of the signal and a consequent error on harmonic analysis (which will be the greater, the less accurate is the signal reconstruction). Limiting such errors is needed for obtaining a more accurate information, within the Standards error limits [1]-[2]. From a practical viewpoint, the implementation of harmonic analysis algorithms on low-cost devices is also a topical issue for PQ measurements; for typical smart metering platforms the optimization of the processing algorithm is crucial to perform the analysis in a short time and to limit the costs related to the hardware components. The FFT is obviously the most suitable algorithm (if compared to DFT); thus, it is necessary to find the best solutions for its implementation in low-cost devices, keeping errors within the limits imposed by the Standards.

In this framework, the aim of this paper is to analyse the performances of harmonic analysis implementation using FFT with different interpolation algorithms and sampling rates. The final aim is to demonstrate how these aspects can impact on the choice of the measurement device and its technical features. The paper is structured as follows: firstly, target measurement issues are considered for harmonic analysis. Secondly, a simulation study is presented to verify analytically how the considered issues impact on harmonic analysis. Finally, to verify the measurement issue impact in a real case implementation, some experimental tests are presented, which have been carried out with two different commercial data acquisition boards.

II. HARMONIC ANALYSIS MEASUREMENT ISSUES

The IEC 6100-4-7 standard imposes limits on the accuracy of harmonics for Class A instruments [2]. For the measurement of voltage harmonics, the Standard provides two different conditions that must be respected, depending on the amplitude of the harmonic measured U_m:

$$\text{Cond. 1: } U_m \geq 1\%\, U_{nom} \rightarrow e < \pm 0.05\, U_m \qquad (1)$$

$$\text{Cond. 2: } U_m < 1\%\, U_{nom} \rightarrow e < \pm 0{,}0005\, U_{nom} \qquad (2)$$

where U_{nom} is the voltage rated value.

The error in measuring the amplitude of the individual harmonics depends on how accurately the single harmonic is detected within the harmonic spectrum.

According to IEC 61000-4-30, the observation window (T_w) must be equal to 200 ms, i.e. 10 cycles of the fundamental frequency at 50 Hz [1], [9]; a maximum synchronization error is allowed of 0.03% of T_w; when such condition is not met, Hanning window can be applied. This may reduce the scallop loss errors in harmonics amplitudes measurement, while it does not have effect on frequencies measurements, unless further processing is made on spectrum samples (such as a frequency domain interpolation). To synchronize the sampling, the IEC 61000-4-30 require a preliminary measurement of the signal frequency; after this, sampling frequency f_s and number of acquired samples n can be set [10], [11]. In this viewpoint, a high sampling frequency allows acquiring more samples in the same T_w and to have a more accurate reconstruction of the signal. However, the processing of a high number of samples can be a problem for low-cost devices, in terms of memory and computational capabilities (to allow obtaining the measurements within the specified time constraints).

As regards the sampling synchronization, usually data acquisition system uses a fixed sampling frequency. This is the case of typical platforms for smart metering purposes, where f_s value is normally obtained by scaling the on-board clock frequency. This may lead f_s to be not suitable for acquiring a number of samples n equal to power of 2 in the considered observation window Tw. A possible solution is to apply an interpolation algorithm to the acquired samples (n), so to obtain the desired number of "interpolated" signal samples (N, equal to a power of 2) and enable the efficient FFT calculation, whatever f_s and n are. However, this introduces an approximation error on the acquired waveform reconstruction. In fact interpolation algorithms act approximating the part of signal between two consecutive points with a given function; their accuracy increases with the order of the approximation function and the number of samples n in the given Tw. So, the accuracy of the signal reconstruction will depend on both f_s, n and the chosen interpolation algorithm. On the other hand, as the order of the interpolation function increases, the computational cost necessary to implement the algorithm increases too.

To evaluate the effects of these parameters on the errors produced by the signal approximation, some case study results (of both simulation and experimental tests) are shown in the following sections.

III. SIMULATION TESTS

Simulations were performed using a LabVIEW software. A Virtual instrument (VI) has been built whose block diagram is shown in Fig. 1; it allows comparing the errors produced by the three proposed interpolation algorithms, in different sampling frequency conditions. In detail, the signal (sum of the fundamental component and its harmonics) is simulated with given sampling parameters (f_s and n, with $n/f_s = T_w$ and $n \neq$ power of 2); then it is interpolated with different algorithms (linear, quadratic and cubic) to obtain the 2-power number of samples (N). The interpolated signal is then processed by FFT. The values of the spectral components are compared with the set values of the individual harmonics (represented by the red arrows in Fig. 1) in order to evaluate the amplitude errors.

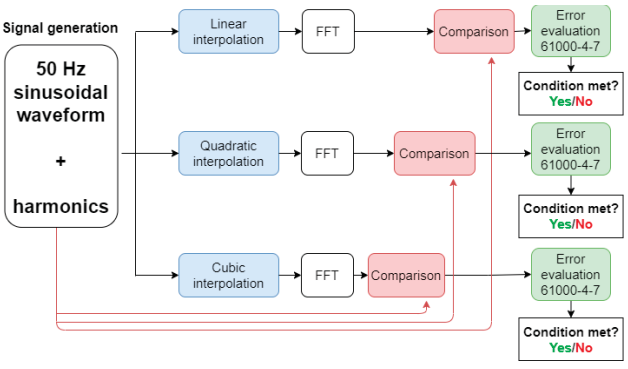

Fig. 1. - Block diagram of the VI used for simulations

Depending on harmonics amplitudes (higher or lower than 1%, see Cond. 1 or Cond. 2 reported above), the VI assesses whether the error limits are fulfilled or not. Since the IEC 61000-4-30 does not give any indication of the test waveform, the test signals used for the simulations were chosen in accordance with the standard IEC 50160 "Voltage characteristics of electricity supplied by public distribution systems" [12], [13]. The test signal had a fundamental frequency of 50 Hz, amplitude of 230 V RMS and added harmonics up to 50th order, with variable amplitudes as summarized in Table 1. The IEC 6100-4-7 imposes that limits on the accuracy of harmonics measurement for Class A must be fulfilled up to the 50th order harmonic; since IEC 50160 provides indications for harmonics up to the 25th, higher order harmonics were added according to the following scheme, similar to IEC 50160, as shown in Table 1:

- Even order harmonics: 0.5% of the fundamental;
- Odd order harmonics: 1.5% of the fundamental.

Simulations were carried out for three different sampling frequencies (f_s = 16, 24 and 32 kHz) and for three different interpolation algorithms (linear, quadratic and cubic). For each case study, the compliance has been verified with the error limits on harmonic analysis imposed by the Standard IEC 61000-4-7. The simulated cases are summarized in Table 2. The signal has an observation window T_w of 200 ms, according to IEC 61000-4-30 and IEC 1000-4-7. The number of signal samples n is given by:

$$n = f_s \cdot T_w \quad (3)$$

Table 1 - Harmonic components amplitude - IEC 50160

Even order harmonics		**Odd order harmonics**			
		three multiples		**no-three multiples**	
Order *h*	Relative amplitude *uh*	Order *h*	Relative amplitude *uh*	Order *h*	Relative amplitude *uh*
2	2,00%	3	5,00%	5	6,00%
4	1,00%	9	1,50%	7	5,00%
6...24	0,50%	15	0,50%	11	3,50%
		21	0,50%	13	3,00%
				17	2,00%
				19, 23, 25	1,50%
uh is the amplitude of the h-order harmonic relative to the amplitude of the fundamental component					

For interpolation and FFT calculation, N equal to 2048 or 4096 has been considered. The errors made with the different algorithms were compared with the IEC 61000-4-7 limit (according to *Cond.* 1 or *Cond.* 2, if measured harmonic amplitude is higher than 1% of the nominal voltage or not, respectively - see Section II). Results of two cases are reported in Fig. 2 and Fig. 3, for f_s equal to 16 kHz and 24 kHz, respectively (N = 2048).

Table 2 - Simulated cases

Case 1: f_s. = 16 kHz	n = 3200	N=2048 N= 4096
Case 2: f_s. = 24 kHz	n = 4800	N=2048 N= 4096
Case 3: f_s. = 32 kHz	n = 6400	N=2048 N= 4096
f_s. = sampling frequency; n= acquired samples; N = number of samples after the interpolation.		

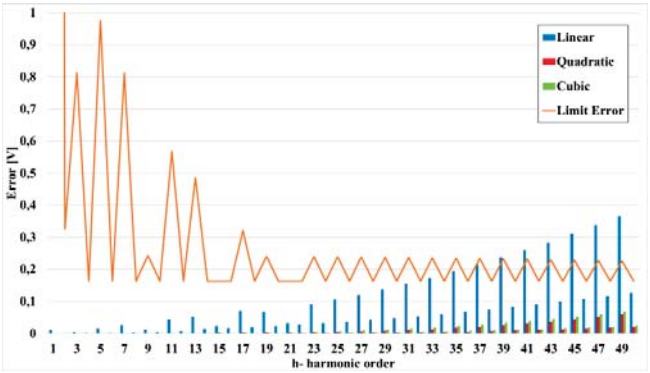

Fig. 2 – Simulation results; f_s = 16 kHz; interpolation with N = 2048 samples

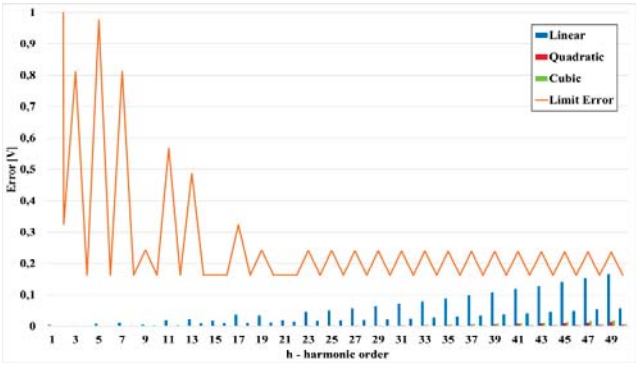

Fig. 3 - Simulation results; f_s = 24 kHz; interpolation with N = 2048 samples

Table 3 – Simulation results; compliance with IEC61000 4-7 limit errors

f_s. *[kHz]*	*16*	*16*	*24*	*24*	*32*	*32*
N	***2048***	***4096***	***2048***	***4096***	***2048***	***4096***
Linear interpolation	*Not verified*	*Not verified*	*Verified*	*Verified*	*Verified*	*Verified*
Quadratic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*
Cubic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*

In Fig. 2 it is possible to see that the error exceeds the limits in the case of interpolation with linear algorithm;

therefore, the adoption of this algorithm does not allow fulfilling the Standard requirements. On the contrary, as shown in Fig. 3, with a higher sampling frequency, the error is lower for all interpolation algorithms, including the linear one. The same results are obtained by interpolating at N = 4096 samples. Table 3 summarizes the results obtained. Cases where the error condition is not met are highlighted in red; cases when the error condition is met are highlighted in green, instead.

IV. EXPERIMENTAL TESTS

In order to validate the results previously obtained in simulation with an ideal signal, experimental tests were carried out using a real signal. The scheme of the test system is shown in Fig. 4. The signal was generated by using a Fluke 6100-A calibrator and it was acquired with a data acquisition board (DAQ). The generated signal is sampled at a given f_s and then it is interpolated with the different algorithms (linear, quadratic and cubic) to obtain the 2-power number of points N. Each interpolated signal is then processed by FFT. The values of the spectral components are compared with the respective values set on the power calibrator, in order to evaluate the errors (i.e. the power calibrator values were assumed as reference for errors evaluation).

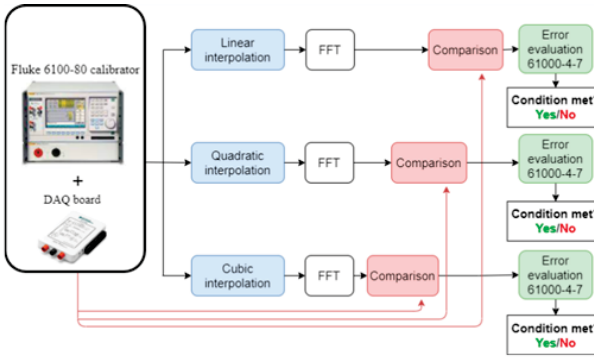

Fig. 4 - Scheme of the measurement setup and VI used for experimental tests

The tests were carried out with two DAQs, to compare the results obtained with different devices and ADC resolutions. The first board is a NI myDAQ board, which has a maximum sampling rate of 200 kHz, an input voltage range of 10 V and a 16-bit ADC. The second board is a NI 9252 board with 24-bit ADC, a maximum sample rate of 50 kHz and an input voltage range of 10 V. The test signal was a signal with a fundamental component (frequency 50 Hz, rms 7 V) and all harmonics up to the 50th, with amplitudes according to Table 1. For the tests with NI myDAQ the same sampling frequencies of previous simulations tests were used (16, 24 and 32 kHz). For NI 9252 the sampling frequency can be set according to the formula $f_s = \frac{f_M}{128 \cdot a}$, where a is an integer number (2,3,4….) and f_M is the DAQ Internal master time base (12.8 MHz). Thus the tests were carried out with signal frequencies of 16.67 kHz, 25 kHz and 33.34 kHz, (respectively for a=3, 4 and 5), in order to use the nearest possible values to those used for simulations and experimental tests with NImyDAQ. For both DAQs, the errors made with the different algorithms were compared with the limit imposed by the standard (as made for simulations). Ù

The errors results for the three interpolation algorithms are shown in Fig. 5 and Fig. 6 (for the NImyDAQ and the NI 9252, respectively). For the lowest sampling frequency, in both cases the errors made with the linear algorithm exceed the IEC 6100-4-7 limits, even if is visible that, with the same algorithm and number of interpolated points, the errors obtained with the NI 9252 board are lower than those obtained with the NImyDAQ (due to the better accuracy specifications). On the other hand, the error limits are fulfilled with both DAQs for the other tested sampling frequencies.

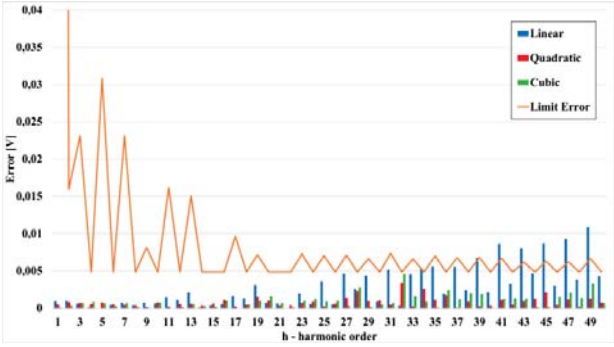

Fig. 5 – Experimental results - NImyDAQ, fs = 16 kHz; interpolation with N = 2048 samples

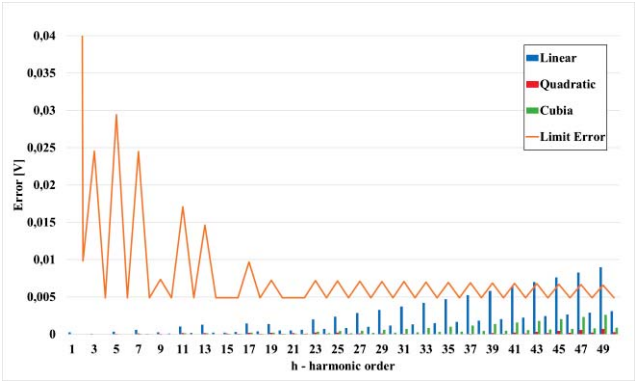

Fig. 6 - Experimental results - NI 9252, f_s = 16.67 kHz; interpolation with N = 2048 samples

Table 4 summarizes the results obtained in all tests. Cases where the error condition is not met are highlighted in red; cases where the error condition is met are highlighted in green, instead. As can be seen, the experimental results are in accordance with the simulations, even considering the different DAQs

accuracies. For the lowest value of f_s (around 16 kHz) the linear interpolation algorithm does not allow to meet the IEC 6100-4-7 limits) for both DAQs and both values of N (2048-samples and 4096-samples interpolation). For all tested sampling frequencies, results within the IEC 6100-4-7 limits were obtained with the quadratic and cubic algorithms, instead.

Table 4 – Experimental results; compliance with IEC61000 4-7 limit errors

NImyDAQ						
f_s. [kHz]	***16***	***16***	***24***	***24***	***32***	***32***
N	***2048***	***4096***	***2048***	***4096***	***2048***	***4096***
Linear interpolation	*Not verified*	*Not verified*	*Verified*	*Verified*	*Verified*	*Verified*
Quadratic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*
Cubic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*
NI 9252						
Linear interpolation	*Not verified*	*Not verified*	*Verified*	*Verified*	*Verified*	*Verified*
Quadratic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*
Cubic interpolation	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*	*Verified*

V. PRELIMINARY ANALYSIS ON COMPUTATIONAL COST

In addition to the impact on harmonic analysis results, the choice of the interpolation function determines also an impact on the overall computation cost of the processing algorithm. Thus, it must be made considering the computational capabilities and performances of the hardware device where the algorithm is meant to be implemented. In fact, the higher the order of the interpolation function, the higher the number of operations needed to perform the interpolation. For a given value of N, the cubic interpolation (third-order polynomial function) will require an higher computational burden than the quadratic one (second-order polynomial function), which in turn will require an higher computational burden than the linear interpolation (first-order polynomial function), Depending on the processing capabilities of the hardware device, this implies more time required to perform all operations and, in some cases, the interpolation implementation can be not feasible, especially in low-cost devices (with limited memory, speed and computational features).

For example, the operations required for each interpolation algorithm (linear, quadratic cubic) are reported in Table 5, for both cases of N = 2048 and N = 4096 points. The total number of required operations for the harmonic analysis computation is given by the sum of interpolation and FFT algorithms operations. It should be noted that the number of operations does not depend on the sampling frequency but only on N value.

Table 5 – Computational cost. Number of operations vs. interpolation algorithm

		Number of operations		
		FFT	**Interpolation algorithm**	**Total**
N = 2048	Linear Algorithm	22528	12288	34816
	Quadratic Algorithm	22528	45056	67584
	Cubic Algorithm	22528	65536	88064
N = 4096	Linear Algorithm	49152	18432	67584
	Quadratic Algorithm	49152	90112	139264
	Cubic Algorithm	49152	131072	180224

CONCLUSIONS

This paper has presented a study on the effectiveness of time-domain interpolation algorithms for the implementation of harmonic analysis on common smart metering platforms, according to IEC 61000-4-7. The study has investigated the feasibility of using such algorithms when the meter sampling frequency does not allow to obtain the synchronous observation window with a suitable number of acquired samples for the efficient FFT implementation (i.e. equal to a power of 2).

The study has been aimed at evaluating how sampling frequency and the interpolation algorithm used for the implementation of FFT can affect the error on harmonics measurement. Different case studies have been analysed and compared, in order to study the impact of the sampling frequency and interpolation function (linear, quadratic and cubic) on both spectral analysis accuracy and algorithm complexity. Actually, a suitable trade-off between such features is crucial for the implementation of PQ measurements, according to IEC 61000-4-30 ad 61000-4-7, even in low cost devices, keeping the errors on harmonics measurement below the limits imposed by such Standards. To reach the performances of the highest accuracy class (Class A) is mandatory to use high efficiency but not complex solutions, to limit the need for expensive hardware components, without worsening the measurement accuracy.

Different simulations were carried out both in LabVIEW environment with an ideal signal and with a real signal acquired with DAQ boards. The results show that, with a given sampling frequency, it is not always possible to use the linear interpolation algorithm, so it is necessary use more complex algorithms, with higher computational cost. This could be not feasible for a commercial device, depending on its speed, computation and memory capabilities. This will result in the need for more powerful data acquisition systems and more memory capabilities for the storage of acquired samples Alternatively, when it is possible to increase the sampling rate, simpler interpolation algorithm can be used (as the linear one).

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