Design of digital sampling impedance bridge for battery impedance spectroscopy

Stanislav Mašláň[1]

[1]*Czech metrology institute, Okružní 31, 638 00 Brno, smaslan@cmi.cz*

Abstract – **The paper describes design of a digital sampling impedance bridge dedicated for battery impedance spectroscopy. It suggests topologies capable of measurement of sub-milliohm impedances in full complex plane. Paper also shows measurement uncertainty contributions of the digitizer nonlinearity and coaxial network of the bridge including parasitic inductive and capacitive couplings in the network. Combined uncertainty of the bridge with common NI 9238 digitizer ranges from less than 20 μΩ/Ω to order of 0.01 % for voltage drop above 1 mV at the measured standard in a frequency range 0.01 Hz to 5 kHz. Angular errors can be as low as 1 μrad for frequencies below 1 kHz when measured voltage drops exceed 10 mV. The paper also presents experimental measurements showing capability to measure low impedances from 0.01 Hz to 5 kHz.**

I. INTRODUCTION

Digital sampling impedance bridges, which are well suited for low impedance measurements, are being used for over 20 years in various topologies. Extensive review of metrology grade low impedance bridges is shown e.g. in [1]. However, vast majority of the bridges is designed for measurement in audio frequency range and without presence of DC bias voltage. Electrical Impedance Spectroscopy (EIS) of batteries however requires somewhat unusual operating conditions. First, the frequency range of interest often lies well below 1 Hz which brings several problems. One of them is equalization of currents in coaxial network. At higher frequencies it can be enforced by use of coaxial chokes. At low frequencies the chokes have almost no effect, so different methods must be used. Next, the EIS meters operates in presence of DC bias voltage. Unlike for higher frequency measurements it is not possible to simply use AC coupling of the digitizer. Thus the AC voltage drop at the standard (UUT) is typically digitized together with DC bias, which results in digitizing high DC voltage and comparably small AC voltage drop proportional to the impedance of UUT. This significantly limits resolution of digitizer and thus achievable uncertainty of measurement. Another problem related to precision metrology of low impedance in presence of DC bias voltage is lack of other precision reference measurement methods. Thus the uncertainty of such bridge and its vali-
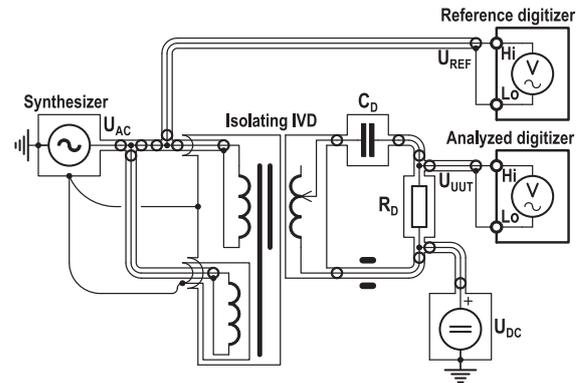

Fig. 1. Connection for analysis of digitizer linearity in presence of DC bias voltage.

dation can be performed only on basis of numerical modelling of measurement network. Mentioned challenges are addressed by new EMPIR [2] project "Lithium Batteries for Second Use" [3]. Following paper shows possible approach to the design of such impedance bridge using few unusual techniques.

II. ANALYSIS OF DIGITIZER LINEARITY

Before design of the bridge started, it was necessary to select digitizer and evaluate its errors under the expected operating conditions. For simplicity the popular digitizing multimeters 3458A [4] were selected as a first choice digitizer, because they are quite abundant in many labs.

Numerous authors performed precision characterization of these digitizers. Possibly most comprehensive characterisation is shown in [5]. However, such analyses were always limited to either DC linearity or dynamic AC linearity with relatively high voltage without presence of large DC bias. In case of EIS bridge it is relevant to evaluate performance of the digitizer in presence of DC bias up to at least 5 V with AC voltage component even below 1 mV. One of the required features of the bridge is insensitivity of its impedance measurement error on the DC bias voltage. To validate this, a simple test circuit according Fig. 1 was designed. An isolating inductive voltage divider (IVD) with one decade and excitation winding was built. Output of the IVD was connected to an impedance CR divider formed of a calculable resistor $R_D = 1 \text{ k}\Omega$ and air capacitor $C_D = 1 \text{ nF}$. These can be calibrated easily down to order of

few parts in 10^6 uncertainty. Therefore, the combination of IVD and CR divider enables generation of small AC voltage with relative uncertainties far below $10 \, \mu V/V$ on both inphase and quadrature components up to at least 1 kHz, which is more than sufficient for this purpose. Variable DC voltage U_{DC} is added to the output of the divider via a low potential terminal of reference resistor R_D so the AC and DC components can be controlled independently. Input voltage U_{REF} of the IVD is digitized by reference digitizer and it is used only as a level and phase reference for evaluation of the UUT voltage U_{UUT} measured by the analyzed digitizer. Both digitizers and synthesizer (National instruments DAC NI 9260) were phase locked, so coherent sampling was achieved and thus simple FFT with rectangular window was used to evaluate the voltage vectors U_{REF} and U_{UUT}.

The rms AC voltage applied to the UUT was chosen to be an extreme case - only $100 \, \mu V$ which may represent $100 \, \mu\Omega$ impedance measured with AC current of 1 A. U_{DC} was varied from zero to 5 V with UUT digitizer set to 10 V range. The AC voltages measured by UUT were compared to calculated values of generated AC voltage U_{UUT}. Experiment was repeated for various aperture times of the Keysight 3458A and absolute errors are shown in Fig. 2. For very long aperture of 3 ms the absolute AC errors were below $0.1 \, \mu V$. However, for shorter apertures needed for higher measurement frequencies the random jumps appeared at some DC biases. Note the errors are not caused by noise - they were repeatable although different for each tested 3458A unit.

The same test was also repeated with a new digitizing multimeter Fluke 8588A [6]. Possibly due to its low resolution AD converter (18bit), the measurements were much noisier than with 3458A so much longer measurement times were needed to reach comparable type A uncertainty. Processed results are shown in Fig. 3. As expected no difference in AC errors was observed for various aperture times, because this DMM uses fixed resolution AD converter instead of integrating type and it emulates aperture time by simply averaging subsequent samples. The largest observed errors were about one quarter of 3458A's, but still significant.

Just for curiosity the same experiment was repeated with 24bit digitizer NI 9239 [7] from National Instruments with input voltage range of ± 10 V. Result is shown in Fig. 4. This digitizer performed unexpectedly well. The observed errors were mostly below $0.1 \, \mu V$ in full range of DC bias at full sampling rate of 50 kSa/s for all tested AC voltages. Therefore this digitizer is also possible candidate for the EIS bridge. Furthermore, is has low input capacitance, low capacitance to ground and four fully floating inputs, so one unit is sufficient for a whole bridge.

Under assumption the measured voltage drop will be e.g. 1 mV (1 mΩ impedance at current 1 A), the 3458A unit er-
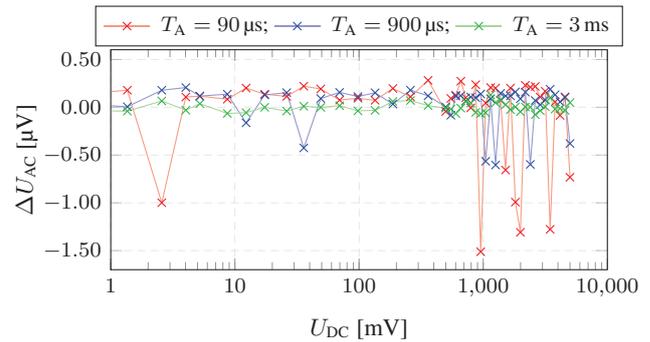

Fig. 2. Absolute error of 3458A AC voltage measurement as function of DC voltage for various apertures T_A. Range: ± 10 V, sampling mode: "DC V", applied rms AC voltage: $100 \, \mu V$ and 16 Hz. Expanded uncertainty was approx. $0.06 \, \mu V$ for all spots.
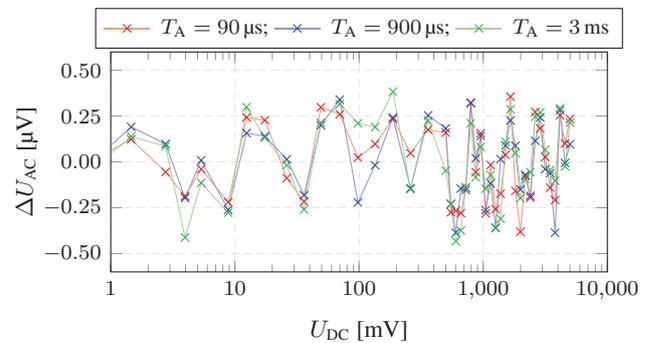

Fig. 3. Absolute error of Fluke 8588A AC voltage measurement as function of DC voltage for various apertures T_A. Range: ± 10 V, measurement mode: "Digitizing", applied rms AC voltage: $100 \, \mu V$ and 16 Hz. Expanded uncertainty was approx. $0.15 \, \mu V$ for all spots.
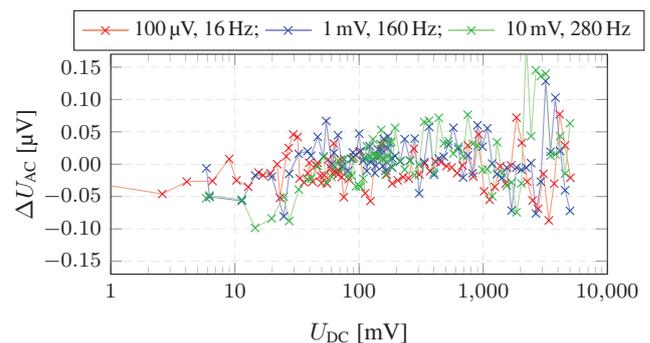

Fig. 4. Absolute error of NI 9239 AC voltage measurement as function of DC voltage for various applied rms voltages. Expanded uncertainties for particular AC levels were {0.06; 0.06 and 0.2} μV.

rors will lead to approx. 0.01 to 0.2 % relative uncertainties just because of its nonlinearity. Fluke 8588A can provide 0.05 % relative uncertainty for a cost of very long measurement times and NI 9239 can provide uncertainty below 0.015 %.
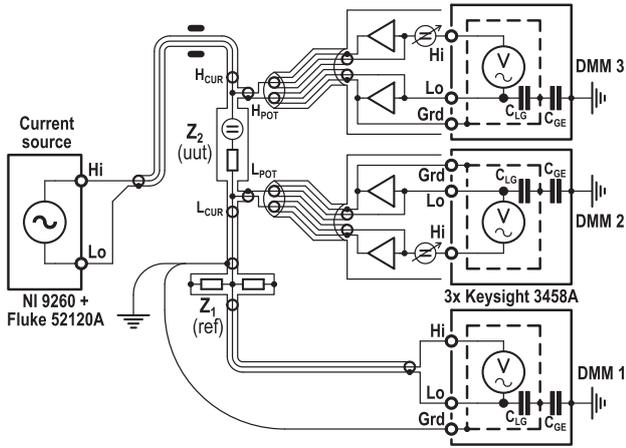
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Fig. 5. *Connection of 4TP digital sampling impedance bridge for battery EIS.*

Another set of linearity tests was performed for a case of measurement without presence of DC bias. Example of AC linearity for sampling multimeter 3458A obtained by linearisation technique described in [8] is shown in Fig. 6. The 3458A multimeters in general provide excellent AC linearity when operated above 10% of range, however below the threshold the nonlinearity builds up and can have very random shapes among various 3458A units. The shape also starts to change above some 300 Hz. The linearity also improves when longer aperture time is selected. Although experiments showed the linearity shape changes even in matter of days, it seems to be restored by AUTO-CAL DCV procedure of the DMM to order below 10^{-6} which is perfectly sufficient for this impedance bridge. No long term changes after AUTOCAL DCV were observed at least in order of months.

Another test of AC linearity was performed with NI 9238 (± 500 mV version of NI 9239). The linearity obtained by the same method as for 3458A is shown in Fig. 6. The shape seems to be more monotonic compared to 3458A so less density of voltage steps is needed to obtain usable linearity correction. Note the errors of the ultra low voltages shown in Fig. 7 were obtained by use of CR divider with very high ratio similarly as in Fig. 1. Stability of the linearity shape in time was not yet extensively evaluated for this digitizer.

In conclusion the errors of all tested digitizers are sufficient to meet target of EMPIR LiBforSecUse project [3] (1 % expanded relative uncertainty for 1 mΩ measurement), but it is still far from what is expected from a typical impedance metrology grade system, so alternative solutions providing better uncertainties were considered.

III. DESIGN OF THE BRIDGE

Basic requirements for the bridge are following: (i) Measurement of four/five terminal (4T/5T) and four ter-
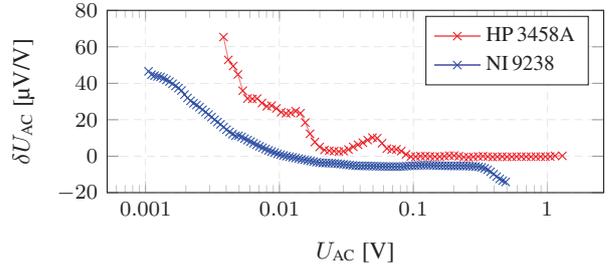

Fig. 6. *Relative error of HP 3458A and NI 9238 AC voltage measurement as function of applied AC amplitude. HP 3458A was configured to range 1 V, sampling rate 5 kSa/s, aperture of 120 µs. NI 9238 was configured to 50 kSa/s. Frequency of test signal was 60 Hz.*
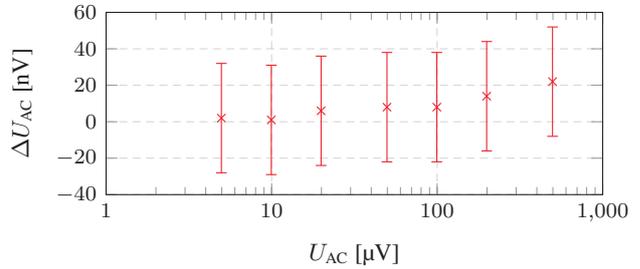

Fig. 7. *Absolute AC voltage error of NI 9238 for ultra low voltages, configured to sampling rate 50 kSa/s, test frequency 60 Hz.*

minal pair (4TP) standards; (ii) Impedance range down to at least 1 mΩ; (iii) Frequency range 0.01 Hz to 5 kHz; (iv) AC+DC supply current; (v) Capability to measure with DC bias voltage at least up to 5 V.

It is evident that several compromises must be made. First, as the target are low impedance standards, it is critical to achieve equalized currents at least in current ports of the UUT Z_2, because even small mutual couplings to the potential cables will cause large errors. However, it is not possible to use coaxial chokes at frequencies well below 1 Hz so other techniques must be used. Second, it is not possible to use any transformers, so the traditional Kelvin arm with injection transformer is also not possible. Thus, the straightforward solution shown in Fig. 5 was considered. This solution is based on simulations using Spice circuit models that were designed to evaluate measurement errors of various topologies. The models contain approximate models of the used components based on their impedance characterization. It even implements parasitic magnetic and capacitive couplings between any pair of cables and ground lugs, so the interference effects arising from imperfect current equalization in the cables are taken into account. The model was combined with Matlab scripts that allow to parametrize the component values and also enable Monte Carlo uncertainty evaluation.

The chosen current source for the bridge is transcon-

ductance amplifier Fluke 52120A controlled by the DDS synthesizer based on NI 9260 24bit DAC [9]. This amplifier can deliver desired currents 2 A AC and 2 A DC (bias). It is able to operate with appliance voltage over 6 V, so it can handle the required DC bias voltage 5 V. The output of the source is connected to the coaxial cable which supplies the H_{CUR} port of UUT impedance Z_2. L_{CUR} port is connected by another coaxial cable to the reference impedance Z_1. The Z_1 was chosen to be a coaxial shunt which is optimal as it can be calibrated and/or modelled to relative uncertainties down to few parts in 10^6 on both inphase and quadrature component. The reference ground of the network is at the Z_1 current input shield, so the digitizer DMM 1 low terminal is at near zero potential. In this connection the currents in the current loop coaxes are almost perfectly equalized with exception of the leakage via the potential measurement cables, so the magnetic interference is minimized even without coaxial choke. However, the small 10 mH choke is placed to the current path anyway as it improves equalization above few hundred hertz.

Any of the tested digitizer models can be used in place of digitizers DMM 1 through DMM 3, however most common type is 3458A which is shown in the circuit. It has benefit of high stability and guarding. Use of NI 9239/9238 would have advantage of using only one unit for all three channels for a cost of possible need to compensate internal crosstalks between its channels and lower gain and phase stability. Main challenge of the design is measurement of potentials at the standards. Z_1 ground potential is near zero, so the leakage via digitizer DMM 1 low-to-ground capacitance is minimized. However, the Z_2 standard has non-zero potential at its case due to voltage drops at current loop cable series impedance. Therefore, there will be always a current flowing via potential cables shields to the large low-to-ground capacitances C_{LG} and C_{GE} of the digitizers. Spice simulation showed these currents can easily cause almost 0.2 % relative errors of the measured impedance of 1 mΩ at 5 kHz.

Elimination of these leakage currents for Z_2 was solved by use of guarding buffers that supply the Guards of the DMM 2 and DMM 3. In order to suppress the errors of DMMs due to the DC bias, it was decided to complement the guard buffer modules by an experimental DC component subtractors. The simplified diagram is shown in Fig. 8. The module simply connects an 18bit floating D/A converter AD 5781 with output buffer in series with the live signal conductor. The DC voltage is set so it eliminates the measured DC voltage component roughly to zero. Voltage resolution is roughly $40\,\mu V$. Therefore the digitizers can be operated at lower voltage range and thus their resolution and signal to noise ratio is improved by a factor of 10 or more. The key aspect of the module design is minimizing the capacitive leakage from live and return coaxial conductors to ground. Thus the whole module is
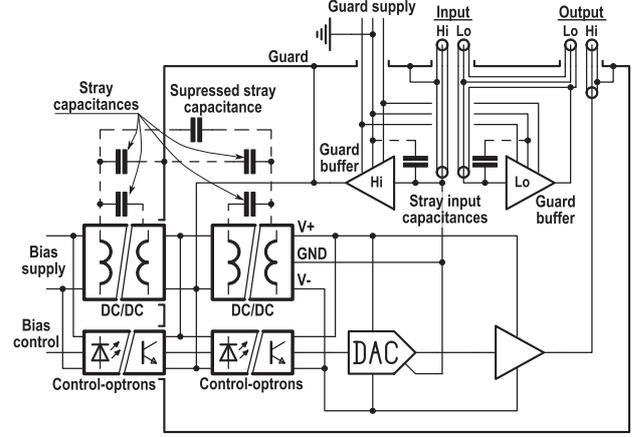

Fig. 8. Simplified connection of DC bias subtraction circuit for EIS bridge.

carefully guarded. As the DC/DC converters used for supplying the floating DAC and buffer have large coupling capacitance, there are two converters connected in series and the joint between them is connected to the guard driver. This way the coupling capacitance from grounded supply to the guarded area is broken. Only remaining capacitances are the guard driver input capacitances and PCB design imperfections, which are below 10 pF in total.

In this topology the four terminal impedance of the UUT is calculated using following equation:

$$\hat{Z}_2 = \frac{(\hat{U}_3 - \hat{U}_2)\hat{Z}_1 \hat{Z}_{IN2}}{\hat{U}_1 \hat{Z}_{IN2} + \hat{U}_2 \hat{Z}_1}, \qquad (1)$$

where $\hat{U}_1$ through $\hat{U}_3$ are measured voltage vectors at particular digitizers, $\hat{Z}_1$ is complex impedance of reference standard and $\hat{Z}_{IN2}$ is input impedance of digitizer DMM 2 including cable and buffer. This equation also partially corrects for the leakage of the measurement current to the DMM 2 from the joint between the standards, which improves accuracy for higher impedances. Another correction that can be applied is loading correction of the potential terminals of Z_1 and Z_2, however at 5 kHz the loading error is still negligible compared to other sources.

The problem of topology from Fig. 5 is DMM 2 and DMM 3 measuring voltage drop at Z_2 operate with common mode voltage given by voltage drop at Z_1 (hundreds of millivolts) and comparatively low voltage difference. Therefore, any difference in gain, phase or linearity between DMM 2 and DMM 3 leads to high errors of measurement when very low impedance Z_2 is measured (low voltage difference between H_{POT} and L_{POT} of Z_2). Although it it possible to correct linearity of digitizers, it is time consuming process with limited accuracy and time stability. Therefore, the topology was experimentally modified according to Fig. 9. In this topology the H_{POT} and L_{POT} port voltages are not measured directly. Instead the four termi-
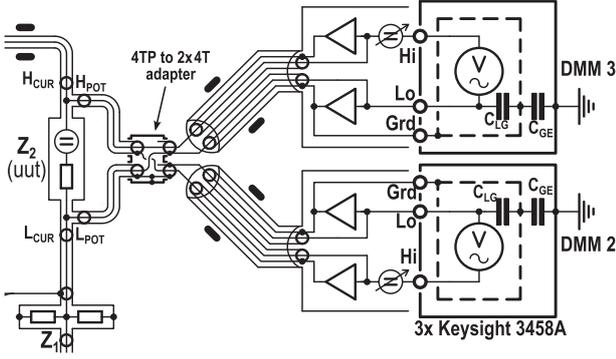
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Fig. 9. Modification of 4TP battery EIS digital sampling impedance bridge for 4T/5T measurement and 4TP measurement in differential connection for very low impedances.
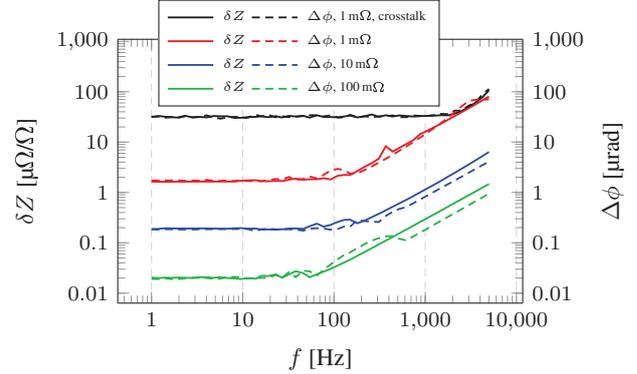

Fig. 10. Calculated expanded uncertainty of the topology according Fig. 9 for different Z_2 values (not including digitizer linearity and reference standard calibration uncertainty). The "1 mΩ crosstalk" simulation was performed with crosstalk contribution included.

nals of the coaxial ports H_{POT} and L_{POT} are connected via adapter so DMM 3 measures voltage drop $\hat{U}_3$ between live conductors of H_{POT} and L_{POT} coaxial ports, which is ordinary 4T measurement. Second digitizer DMM 2 is measuring voltage drop $\hat{U}_2$ between grounds of H_{POT} and L_{POT} coaxial ports which is basically another 4T measurement, so this method will be called 2x4T mode in following text. The two 4T measurements are combined to equivalent 4TP measurement:

$$\hat{Z}_2' = \frac{\hat{U}_3 \hat{Z}_1 \hat{Z}_{IN3}}{\hat{U}_1 \hat{Z}_{IN3} - \hat{U}_3 \hat{Z}_1}, \qquad (2)$$

$$\hat{Z}_2'' = \frac{\hat{U}_2 \hat{Z}_1 \hat{Z}_{IN2}}{\hat{U}_2 \hat{Z}_{IN2} - \hat{U}_2 \hat{Z}_1}, \qquad (3)$$

$$\hat{Z}_2 = \hat{Z}_2' + \hat{Z}_2'', \qquad (4)$$

where $\hat{Z}_{IN2}$ and $\hat{Z}_{IN3}$ are input impedances of the digitizers DMM 2 and DMM 3 including bias and guarding units and cables. Advantage of this solution is the digitizers are measuring directly voltage drops on Z_2 and its shield, so there is no longer problem of common mode voltage as in case of connection shown in Fig. 5. Uncertainty analysis of the NI 9238 card showed they are capable to measure accurately even at very low voltage drops so it is perfectly realistic to measure impedances in order of microohms in this connection, however it is necessary to consider the crosstalk from DMM 1 channel.

For a final design the NI 9238 digitizer was chosen. The uncertainty calculation of the designed 2x4T topology was performed. Realistic cable models and cable lengths were chosen (up to 50 cm length each) and worst case mutual inductances between each pair of cables were estimated. The inductances varied from few nanohenry up to some 100 nH. As expected, the biggest influence of mutual couplings was caused by interference between potential ports of Z_2 and current carrying cables. They can be suppressed by right angle arrangement of current and potential cables

and also by one additional modification - addition of small 100 μH chokes (single toroidal ring) on the potential cables as shown in Fig. 9 which improved uncertainty above 1 kHz. Obtained results from the Monte Carlo simulation for few typical Z_2 impedances are shown in Fig. 10. Three simulations are shown without the digitizer linearity errors and crosstalk, the forth simulation is including crosstalk effect.

IV. EXPERIMENTAL PERFORMANCE VERIFICATION

Verification was performed using available impedance standards of known values. Reference impedance Z_1 was 200 mΩ coaxial shunt for all following tests. The AC linearity of NI 9238 was corrected in range 1 mV to 500 mV, otherwise the uncertainty of measurement would be limited to at least 50 μΩ/Ω even below 1 kHz. Note even after linearisation the residual nonlinearity became dominant uncertainty source above 1 kHz.

Complex impedance of coaxial shunt of impedance 6 mΩ was measured at current of 1 A as a first test. Measurement was performed in the 2x4T configuration. The bridge reached expanded uncertainty around 30 μΩ/Ω for frequencies below some 1 kHz. Both resistance and reactance deviation stayed well below 200 μΩ in lower frequency band. Next test shown in Fig. 12 was performed with 10 mΩ 4TP coaxial standard at very low frequencies down to 0.01 Hz. Measurement was performed in 2x4T configuration. Relative errors on main component stayed below 0.002 %. Absolute errors stayed below some 0.15 μΩ for both resistance and reactance. Note the reference values of the standard were obtained by model interpolation between DC and LF measurements performed by regular digital sampling bridge as no other method was available in this frequency range. Another test shown in Fig. 13 was measurement of 1 mF 4TP capacitor in 4TP
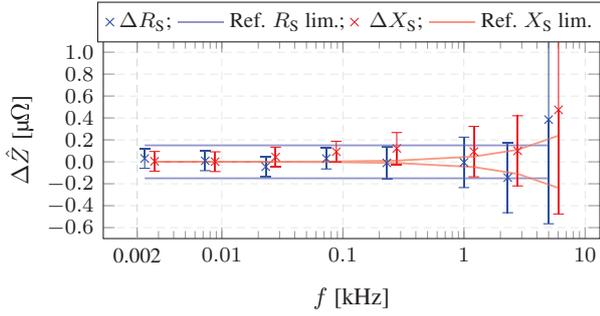
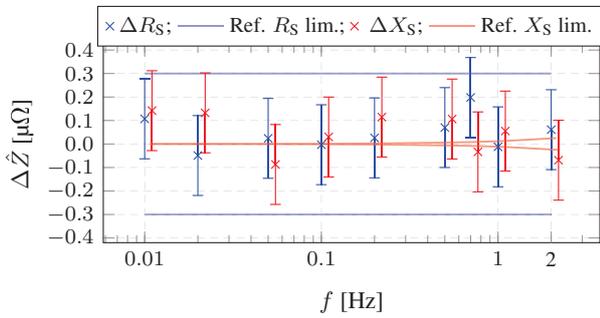*Fig. 11. Absolute deviation of bridge complex impedance measurement when comparing 6 mΩ shunt to a 200 mΩ reference shunt at current 1 A.*

Fig. 12. Absolute deviation of bridge complex impedance measurement when comparing 10 mΩ 4TP resistor to a 200 mΩ reference shunt at current 0.5 A.

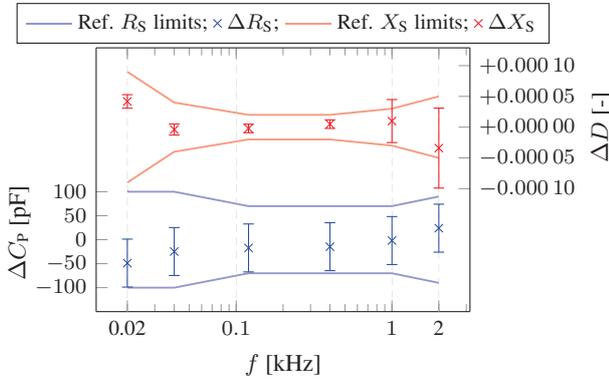*Fig. 13. Absolute error of bridge measurement when comparing 1 mF capacitor to 200 mΩ shunt with current below 100 mA.*

bridge connection. The new bridge provides somewhat better uncertainties than reference digital sampling bridge at low frequencies and comparable or worse above 1 kHz. Note the uncertainty in this experiment was limited by stability of the capacitor.

V. CONCLUSION

Requirements for an impedance analyzer for battery impedance spectroscopy were summarized and possible topologies using digital sampling technique were pro-

posed. Linearity of various suitable digitizers under the expected operating conditions was analyzed and topology modification suggested. Final sampling bridge designs were described. Spice model having realistic component values was prepared and used to evaluate uncertainty of measurement of the bridge. Several practical measurements verifying the bridge capability down to ultra low frequencies were performed.

VI. ACKNOWLEDGMENT

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