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Enhanced fast digital integrator
for magnetic measurements

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Abstract **– An enhanced Fast Digital Integrator (eFDI) was designed to satisfy the new requirements in terms of dynamic accuracy, noise, self-calibration accuracy, and data throughput arising from current on-field exploitation of the previous integrator (FDI) [1] in magnetic measurements for particle accelerators at CERN. In this paper, initially, the specifications, the design solutions, and the main features of the eFDI prototype are illustrated. Then, the preliminary results of the metrological characterization are compared with the FDI performance in order to highlight the achieved improvements.**

I.   INTRODUCTION

FDI was conceived at CERN in cooperation with the University of Sannio for the final tuning of the superconducting magnets bending the particles beams trajectories of the Large Hadron Collider. For this reason, an accurate measurement of the field quality was necessary to suitably control the trajectories as well as to focus the beam [2]. Standard magnetic measurements on accelerator magnets are mostly based on the integration of a voltage signal in order to get the magnetic flux, according to Faraday's law (such as in rotating coils, fixed coils, stretched wire, and so on), complemented also by other techniques (such as Hall plates) [3].

The integrator capability would cover local and integrated field strength, field direction, harmonics and axis for both low and high field conditions. In the rotating coil method, the magnetic flux is measured by a voltage integrator which receives the trigger by an encoder which defines the two angular measurement positions. The Fast Digital Integrator (FDI) [4][5] exploits state-of-the-art sampling rate and resolution digitization: Fig. 1 shows the main FDI specifications.

Due to its characteristics, FDI usage was recently extended to other application areas at CERN. In particular, current state of the art for FDI on-field exploitation shows applications to [9] (i) rotating coils for superconducting magnet testing, (ii) vertical cryostat bench, (iii) resistive magnet testing for linear accelerators (Linac4) [11], (iv) magnetic properties bench, and (v) superconducting cable test [10].

Parameter	Conditions	Min	Typ	Max	unit
ADC RESOLUTION		18			bit
ANALOG INPUT					
Differential voltage range (FS)	$\pm 5\ V$ on each input leg		± 10		V
	$\pm 10\ V$ on each input leg		± 20		V
External trigger source f_t	$f_{ADC} \geq 2 \cdot f_t$	1		250000	Hz
ADC sampling rate f_{ADC}	8 programmable *values**	1		500000	S/s
gain	13 programmable *values***	0.1		100	
DC	FS = $\pm$ 10 V, $\pm$ 2 σ				
Digitizer DNL			1.5		LSB
Integrator INL	30 min, 27 C - 36 C		$\pm$ 7 ppm		
Integrator stability	24 h, 30 C		$\pm$ 3 ppm		
Integrator repeatability	30 min, 30 C		$\pm$ 1 ppm		
gain error	30 min, 27 C - 36 C		0.2 %		
	24 h, 30 C		0.2 %		
offset error	30 min, 27 C - 36 C		17 ppm		
	24 h, 30 C		7 ppm		
AC	$f_{ADC} = 500\ kS/s$, $OSR = 100, f_{in} = 10\ Hz$				
Digitizer SINAD			97		dB
Digitizer SNHR			103		dB
Digitizer THD			-99		dB
Integrator SINAD			108		dB
Integrator SNHR			118		dB
Integrator THD			-109		dB
UTC RESOLUTION			50		ns
THROUGHPUT RATE	CPCI/PXI bus		1		MB/s

Fig. 1. FDI Specifications.

The indications from on-field applications show the weaknesses (or improvement) of the current system. In particular (i) low throughput [6], (ii) low measurement bandwidth, (iii) high noise floor, (iv) lack of on-board memory, (v) self-calibration effectiveness for residual gain and offset errors, and (vi) poor user info.

In this paper, the enhanced Fast Digital Integrator (eFDI) designed in order to satisfy these new requirements is illustrated. In the following, in Section II, the eFDI design concept and the specific solutions are illustrated. In Section III, preliminary experimental results of eFDI characterization are presented with FDI performance comparison.

II.   eFDI CONCEPTUAL DESIGN

In this Section, (i) the basic ideas, (ii) the architecture, (iii) the main improved sections of the e-FDI are illustrated.

A. Basic ideas

The conceptual design of the e-FDI was based on the following main basic ideas:

Optimization of the programmable gain amplifier with higher and logarithmic gains and lower noise floor: with the adoption of new anti-alias filtering for coil-to-adc best matching, composed by low CMRR, offset, noise and

distortion analog parts and new optimized PCB routing; new high performance self-calibration circuit, based on 20 bits/1 ppm INL DAC;

replacement of the compact PCI I/O accelerator with a new device capable of high throughput and DMA operations.
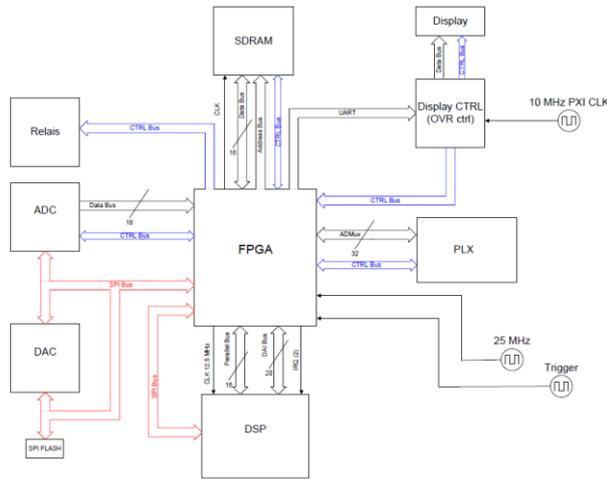

Fig. 2. eFDI Architecture

B. Architecture

Fig. 2 shows the of architecture eFDI. A Field-Programmable Gate Array (FPGA) handles the digital devices, provides the interface for the board bus and acts the real-time ADC operations, providing the selected sampling clock, correlating the digital samples and the very low jitter 25 MHz time stamps; furthermore, it dispatches the SPI bus between the internal memory, the DAC and the Non Volatile Flash; a DSP is in charge of performing the algorithms, carrying out the numerical integration of the samples in the angular domain owing to the trigger pulses of an encoder mounted on the shaft of the rotating coil. The DSP, which is able to communicate directly with the high resolution DAC, is also in charge of self-calibration procedure by selecting all the available gains and ADC sampling frequency and spanning all the input voltage foreseen by the algorithm. Further, the SDRAM allows ADC samples data buffering.
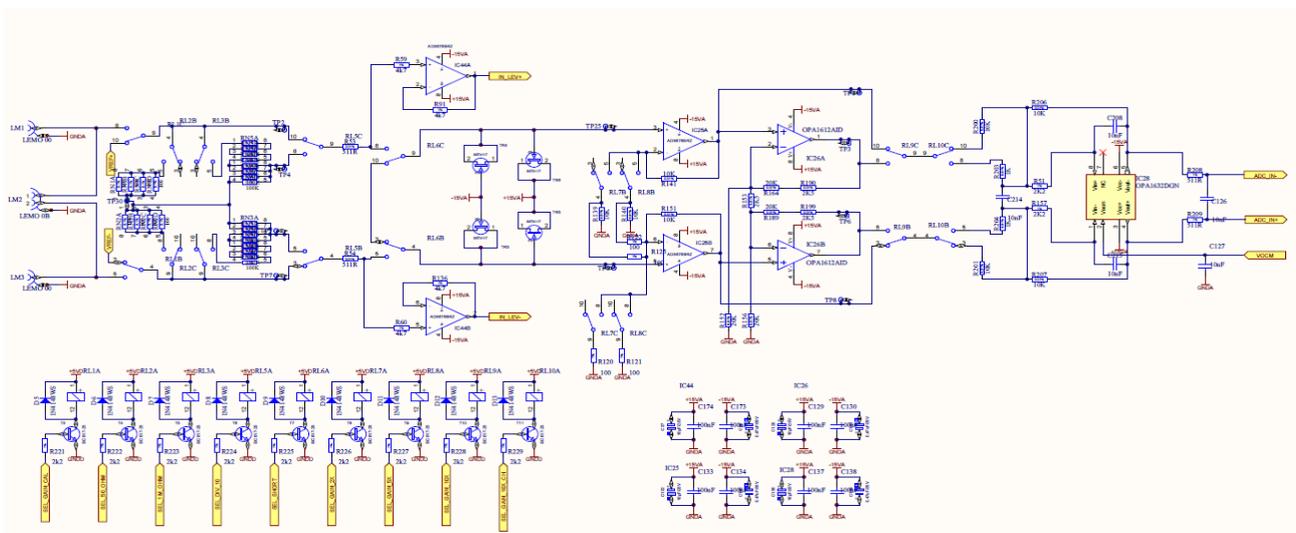
C. Analog Signal Front-end

Basically eFDI has to maintain the same design challenges of the old version: accuracy requirement of 10 ppm for at least 1 s integration time with a bandwidth of 100 kHz [1]. Additionally, a lower noise floor and a best input matching for coil signals have been considered.

Fig. 3 shows the analog front-end design: the ±15 V full scale differential output coil signal is applied, via LEMO connectors, to the input differential stage, which is able to provide 50 Ω or 1 MΩ input impedance and 1/10 or 1/100 division. The 2nd stage is composed by high performance operational amplifiers which configure a Differential Input Differential Output (DIDO) configurable with Gain = 1, 10 or 100. The final stage is based on unity gain, very low noise and distortion, fully differential amplifier, with option gain 10. This stage (i) represents the ADC anti-alias filter, implementing a Butterworth configuration with configurable cutting frequency; (ii) provides the differential reference for the optimized ADC conversion; (iii) allows reducing the noise figure.

D. Self-Calibration

The FDI self-calibration has two main weaknesses. (i)

Fig. 3. eFDI Analog Front End Scheme

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The algorithm is fully handled by FPGA: it makes difficult any changes, due to improvement or bugs, and makes the correction less precise, because of the lack of ALU. (ii) During the calibration steps, the input of the analog front-end is a voltage reference obtained as the output of a resistor network which divides the ±10 V voltage source: it increases the error, which depends on resistor tolerance and ratios, and makes the calibration highly dependent by the temperature despite the adoption of high quality resistors (0.01%).

eFDI self-calibration design is mainly focused to provide high performance voltage references for the

input range: a ±10 V, 1.09 ppm/°C, 6 ppm/1000 h source reference applied, one inverting respect to the each other, to a couple of Analog Devices AD5791 20 bits DAC (1 ppm INL, 0.19 LSB long-term linearity, 0.05 ppm/°C), with no use of resistors on main path, provide the differential calibration signal (Fig. 4).
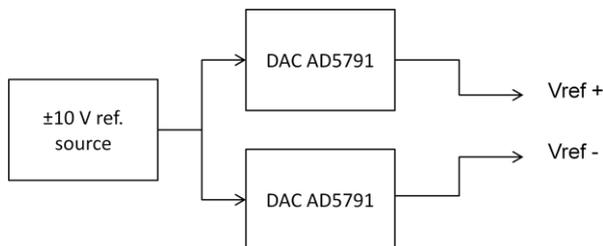

Fig. 4. Self-calibration block diagram

Fig. 5 shows the schematic diagram. The operational amplifiers are used only for signal buffering: the absence of resistor both on source and output signal paths allows providing very high performance and stable input Voltage reference during calibration steps. The two DAC's are directly programmed by the DPS via SPI bus: a large set of Voltage reference are allowed and more effective calibration algorithms are able to be implemented.

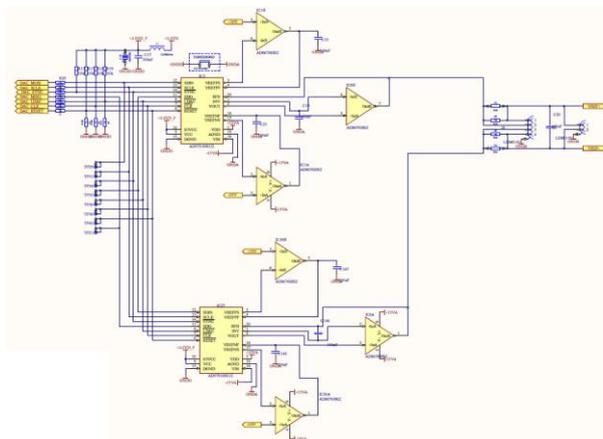The expected offset and gain errors are in the order of tens of ppm.

Fig. 5. Voltage Reference Schematic diagram

E. PXI interface

The PXI (PCI eXtensions for Instrumentation) is a rugged PC-based platform which combines the PCI electrical-bus features with the modular, eurocard packaging of Compact PCI, adding some special synchronization features [7].

FDI is a PXI instrument operating on 32 bits bus at 33 MHz. The theoretical maximum throughput should be 132 MB/s, the measured value results less than 10 MB/s [6]. This is mainly due to (i) system architecture, (ii) single mode access, (iii) no DMA usage, (iv) non optimized device local bus.

The eFDI PXI communication design is based on the most recent PCI9056 HW Accelerator. It is a general purpose mastering device available for generic 32-bit, up to 66 MHz local bus based designs [8]. Fig. 6 shows the system architecture block diagram: (i) device local bus has been optimized and clock frequency increased to 40 MHz, (ii) DMA master mode is allowed for high speed direct data transfer from PC and FPGA internal DPRAM.
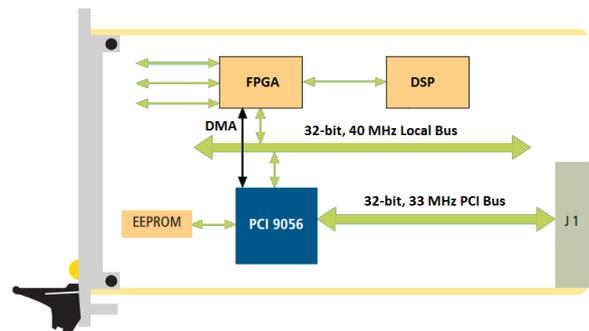

Fig. 6. PXI Communication Block Diagram

III. EXPERIMENTAL RESULTS

Fig. 7 shows the first eFDI prototype realized for testing purposes.

The main performance of the analog front-end and self-calibration has been measured, as well as the data throughput has been tested.

In particular, the resolution of the instrument is estimated by carrying out dynamic tests and evaluating the SINAD (signal to nose and distortion ratio) and the THD (total harmonic distortion). A first set of reported tests aims to assess the performance of the analog chain in different points by acquiring the signals with an external acquisition card. Further tests were carried out to evaluate the prototype acquisition performance by using the on-board ADC. Comparisons of the prototype results with FDI are highlighted, too.

A. Measurement Setup

A metrological station was set up in order to carry out metrological tests on both eFDI and FDI.
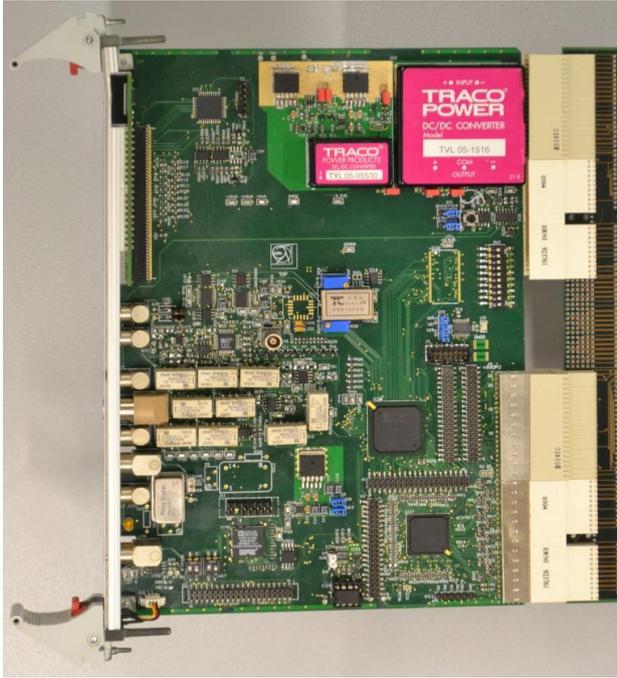
Fig. 7. eFDI Prototype.

The station is based on ADLINK Rack to host the eFDI and one PCI-PXI bridge card, standard PC to host the second PCI-PXI bridge card, STANFORD DS360 calibrator as precision sine generator, NI USB-6289 18 bits data acquisition cards. Software applications were developed in MATLAB.

B. Analog Front-end Tests

A first set of tests, have been carried out to verify the signal degradation along the analog chain: the NI USB-DAQ was applied directly to the dedicated test points (Fig. 3) in order to analyze the analog signal of the amplifier and active filter stages.
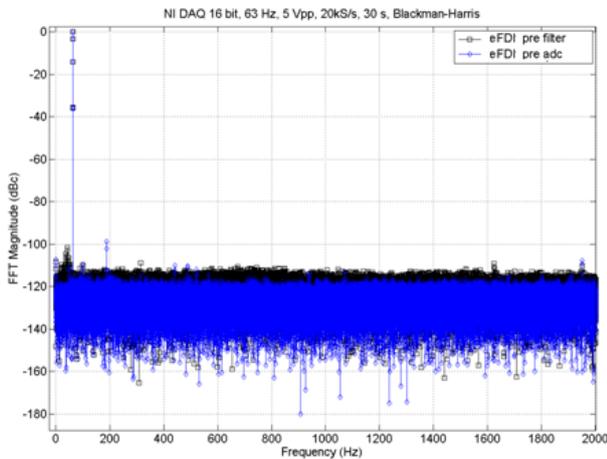

Fig. 8. Amplitude spectrum on pre and post active filter

The tests was performed with a sine wave input, 5 Vpp, at 13 Hz and 63 Hz and the amplifier set to unity gain. The amplitude spectrum of the digitized waveforms at 63 Hz are depicted in Fig. 8. As expected, the noise floor decreases after the low pass filter and the harmonic distorsion, which is not affected by amplifiers, remains constant and more visible since the noise is reduced: the result SINAD is 92 dBc.

During a second set of tests, the performance of the eFDI prototype has been evaluated with the on board ADC by analyzing the raw ADC codes before, showing similar results obtained with the NI DAQ, and then applying an over sampling to finally integrate the over sampled acquisitions.

The over sampling algorithm was implemented directly on the DSP in order to overcame the limits of the data exchange between the card under test and the PC. A set of three different conversion rates was chosen (125, 250, and 500 kS/s) by applying different OSR (125, 250, and 500) in order to have the same resulting sampling frequency. The results (gain 1, 7Hz, 8 Vpp) are shown in Fig. 9. As expected the noise floor decreases by increasing the OSR.
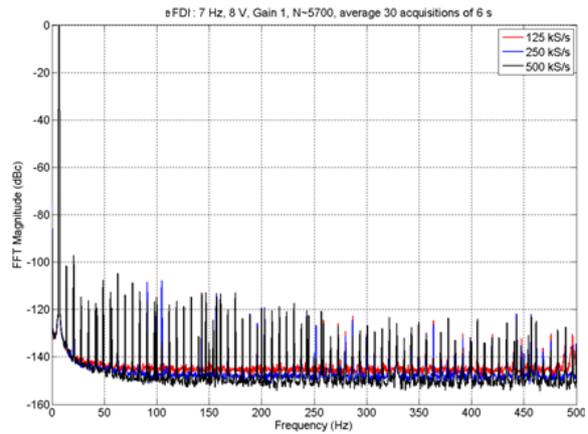

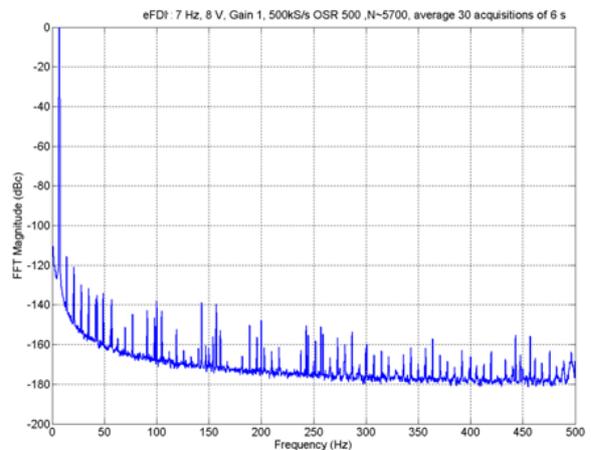*Fig. 9. Amplitude spectrum vs sampling rate.*

Fig. 10. Amplitude spectrum of the integrated data.

Table 1. eFDI performance summary

GAIN	Vpp (V)	f(Hz)	SNR* (dBc)	THD** (dBc)
0.1	30	7.351	101	-95
1	8	7.351	109	-96
10	0.8	7.351	103	-95
100	0.08	7.351	96	-85

*Signal-to-Noise Ratio
**Total Harmonic Distortion

The spectrum of the integrated data is shown in Fig. 10. The SINAD of the instrument used as integrator is 106 dBc and the THD -109 dBc.

C. Self Calibration Tests

To evaluate the new calibration schematic a self-calibration procedure based on linear regression has been implemented.
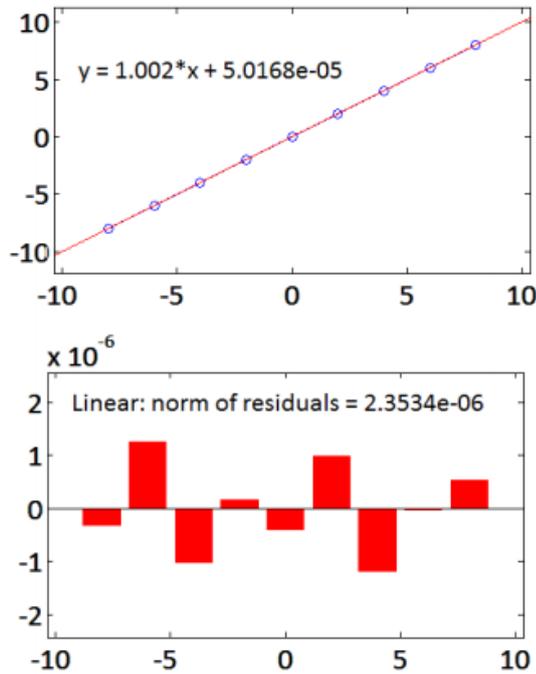

Fig. 11. Self-Calibration linear regression

Fig. 11 shows the gain and offset linear regression and the normalized residual errors measured in the whole analog voltage range. As expected, the error is in the order of 10^{-6}.

D. Throughput Tests

Fig. 12 shows the PLX performance measure of PLXMon, a tool provided by PLX company. The master/DMA operation mode of the PCI9056 provides a suitable throughput (> 100 MB/s) for fast measurement with several integrators (transient analysis of pulsed magnet).

E. Comparison with previous version

Table 2 shows the comparison of three integrator cards: (i) PDI (gain 1000), (ii) FDI with self-calibration (gain 100), (iii) eFDI Prototype (gain 100).
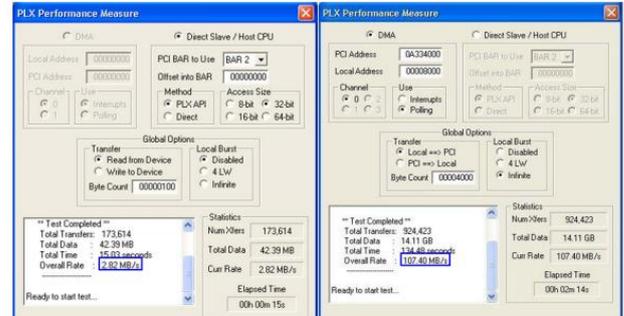

Fig. 12. Comparison between FDI (left side) and eFDI (right side) throughputs

	Gdl (Tm/m)*	STD*	Difference wrt PDI
PDI	50.995	5.02E-04	0
FDI	50.840	4.07E-04	-3.04E-03
eFDI	51.000	4.21E-04	8.87E-05

* average and standard deviation of 5 consecutevely measurements

Table 2. Comparison between PDI, FDI and eFDI

IV. CONCLUSIONS

A preliminary metrological characterization of the first working eFDI prototype was carried out. The analog front-end results are suitable for such a fast and accurate instrument. Reduced noise floor allows signal harmonic analysis also at reduced OSR. Stability vs temperature and time has to be tested. The improved self-calibration procedure provided results comparable with lab calibrated systems. The throughput is highly increased.

ACKNOWLEDGMENTS

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