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Capacitance-to-Digital Converter for Accurate Displacement Measurement in the Sub-nanometre Range

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***Abstract* – This paper presents a capacitance-to-digital converter (CDC) for accurate displacement measurement in the sub-nanometer range. It is intended for applications in metrology, as part of the efforts to create a new transfer standard for length. The main targeted performance characteristics of the CDC are: stability and resolution. Compared with previously reported works, the CDC is optimized with respect to the dynamic range while dissipating only 45 mW of electric power in proximity to the sensor area. The implemented conversion principle uses one resistor, resistance ratio and time as references, thus achieving a good initial accuracy and a very high stability over temperature and time. The interface is realized at PCB level with off-the-shelf components, and measures up to six sensors sequentially. The capacitance measurement range is 9 pF with an option for 18 pF and 32 pF. The resolution of the converter for 9 pF range is 60 aF (~17 bits dynamic range) with less than 2 ms conversion time.**

I. INTRODUCTION

Traceability for length metrology is usually realized via the wavelength of the helium neon laser [1] and optical interferometry. For length measurements with nanometre and sub nanometre accuracy optical fringe division is required making it necessary to correct for small but significant intrinsic errors in interferometers caused for example, by stray reflections, polarization leakage and wavefront curvature. Fabry Perot optical interferometry and x-ray interferometry (XRI) provide two alternative routes to traceability for length measurement. Within the European Metrology Research Programme funded project SubNano, work is being directed towards characterization of capacitance sensors using Fabry Perot interferometry and x-ray interferometry. The x-ray interferometer can be regarded as a ruler or translation stage whose graduations or steps are based on the lattice parameter of silicon which is regarded as a traceable length standard [2]. The silicon d_{220} spacing has an uncertainty of a few parts in 10^8 and use of XRI removes the need for optical fringe division. Capacitance sensors will be referenced against the x-ray interferometer which will generate a known traceable displacement that can be compared to the displacement measured by the capacitance sensor. The configuration will offer the possibility to investigate the sensors performance as a function of angular alignment, working distance and environmental parameters (humidity).

By means of the resonance frequency of an optical cavity, FPI provides sub-nm resolution and convenient direct traceability to the time standard. Displacements are generated through actuation of one of the cavity mirrors while the frequency of a measurement laser is locked to the cavity and tracks the changing resonance frequency. Unlike fringe counting interferometry, this measurement concept is conceptually free of periodic nonlinearity errors. For sensor calibration purposes a suitable reference interface has to be adapted to move together with the actuated cavity mirror. In case of capacitive displacement sensors this has to be a sufficiently flat and smooth target electrode substrate, e.g. a metal coated optical mirror substrate.

In [3], [4] we reported a solution for a capacitive sensor interface that demonstrated very good stability, fast conversion time and a resolution of 14 bits with short cable length [5]. However its power dissipation of ~ 1 W prevents its use in a temperature controlled environment. For this reason, longer cables to the sensor had to be used, which increased the noise and reduced the dynamic range and the stability of the measurement. To solve this problem, a modified version of the electronic interface was reported [6]. It permitted a low power analog front-end circuit to be located close to the sensor, while the actual digital conversion was performed at distance where

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the dissipated heat doesn't affect the sensing area.

Here we present an improved version of the interface, reported in [6], which demonstrates better long term stability by limiting the number of critical components participating in the transfer function of the CDC.

II. THEORY OF OPERATION

The conversion principle is based on the charge balancing technique [4]. An excitation signal is applied to one of the electrodes of the capacitive sensor, while the other electrode is connected to a charge amplifier. The received charge is amplified and stored in an integrator. The integrator is discharged with coarse and fine reference charge generators. The applied reference charge is counted using a charge counter. The value of the counter is incremented with a reference clock frequency by 1 or by 32 respectively when the fine or coarse generators are turned on, thereby representing the sum of the applied reference charge. Knowing the applied reference charge, one can determine the charge received from the sensor and thus its capacitance.

The new features in the presented solution are:

• The input amplifier is separated from the digital converter. After amplification, the analog signal is converted from single-ended to differential, and is transmitted via twisted pair to keep the high power dissipation circuits far from the sensing area.

• For a single conversion, multiple transients of the excitation signal are used. The charge quantities from the sensor are stored in two separate integrators for the positive and the negative transients respectively.

• While the charge from the sensor is being stored in one of the integrators, the other integrator is discharged approximately to zero by applying a known reference charge. Using multiple intermediate discharging cycles instead of one long discharging cycle at the end of the conversion, prevents the integrator from saturating. The effect is as if the integrator was able to be charged to higher voltage, thus increasing the signal value for the particular cycle, which results in improved dynamic range of the conversion.

• When all excitation pulses for the measurement half-cycle are applied and the integrators are coarsely discharged, their residual charge is removed using a single fine discharging cycle. The fine charge generators feed an amount of charge that is 32 times smaller, thereby increasing the resolution of the conversion by an additional 5 bits.

• During the fine discharging cycles, the integrators are disconnected from the input amplifier. This hides the input noise from the output and higher resolution of the conversion is achieved.

• For better stability, a dynamic matching of resistors is used as explained in section III. This ensures, all resistor ratios in the transfer function become independent of production tolerances and temperature variations. As a result, the only remaining reference components in the circuit are a resistor and a quartz oscillator.

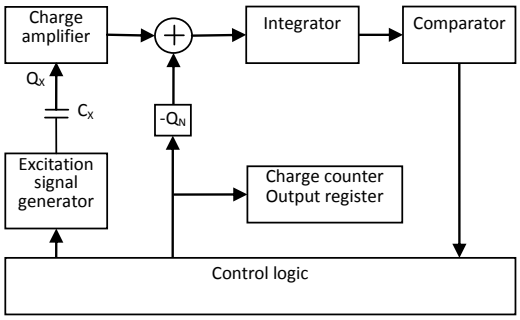

Fig. 1. Block diagram of charge balancing converter

III. IMPLEMENTATION

A. Electrical schematic

The simplified electrical schematic of the analog part of the interface is shown in Fig. 2. The excitation voltage is generated with amplifier A2. The values of resistors R23a, R23b, R23c and R23d are equal and depending on the switches S11, S12, S13 and S14, the gain of A2 can be set to 4, 2 or 1, thus selecting the input range of the converter to 9 pF, 18 pF or 36 pF respectively.

The sensor to be measured is connected to the input amplifier A1 with the switch S1, while the rest of the sensors are grounded to minimize their influence on the measurement.

The output signal of the input amplifier is converted from single-ended to differential using the inverting amplifier A3 and is sent to the converter via twisted pair. The differential signal is applied alternately to the integrators A5 and A8 via the analog multiplexers S5, S6, S7, S8 and the instrumentation amplifiers A4 and A7. The same components are used to implement the function of the coarse charge generators. When coarse discharging of the integrators is needed, the respective instrumentation amplifier is connected to the $-V_{REF}$ and $+V_{REF}$ voltages with the necessary polarity. Because the same components are used for integration of the sensor signal and the reference charge, they don't affect the transfer function, provided that their values are stable for the duration of the conversion.

The fine reference charge generators are implemented with resistors R7, R9 and switches S9, S10. Assuming G_{INA} is the gain of the instrumental amplifier and N_A is the chosen ratio of the coarse and fine reference charge unit, the value of R7 is

$$R_7 = \frac{N_A R_6}{2\, G_{INA}} \tag{1}$$

A similar expression applies for R9, as well. The reason for the factor of 2 is because the fine discharging

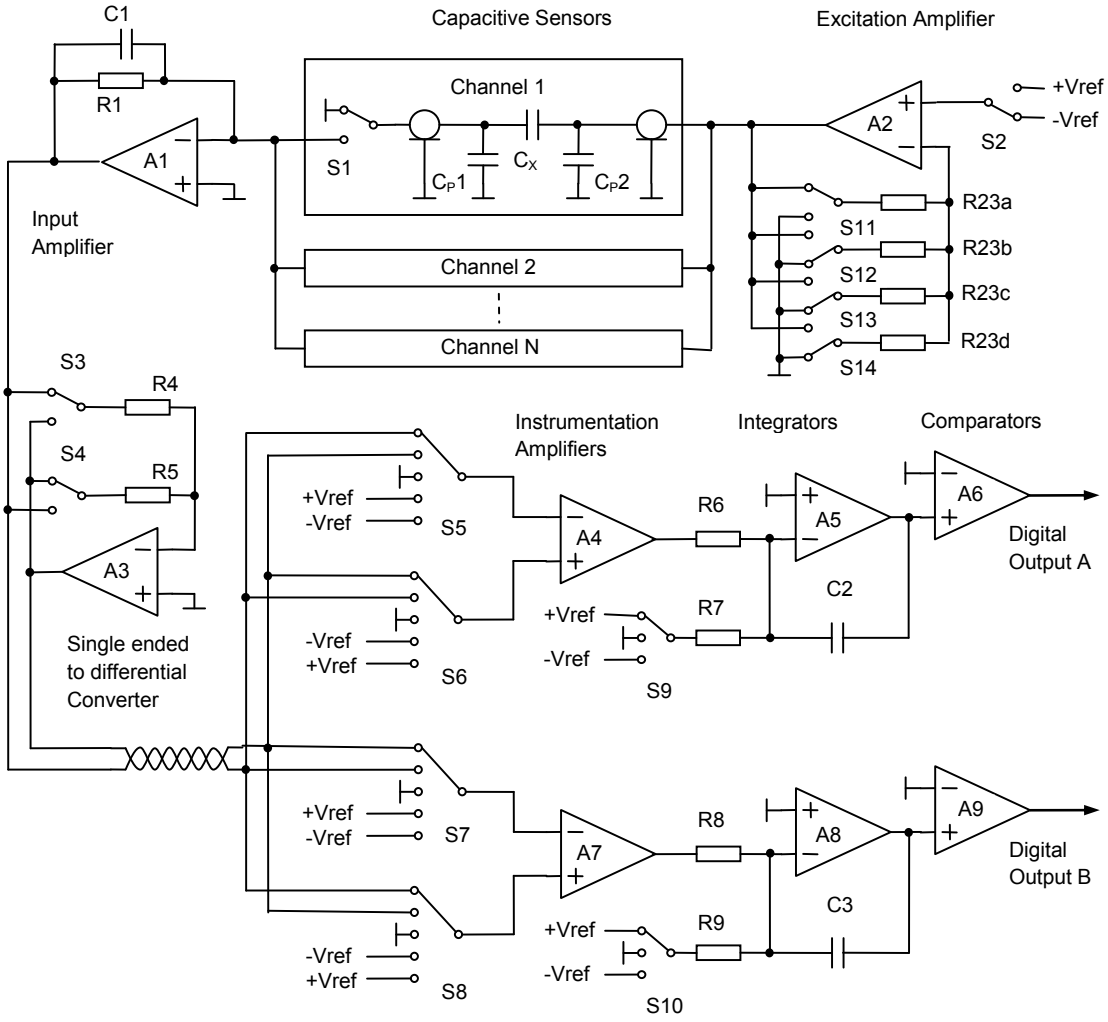

Fig. 2 Electrical schematic of the converter

uses $+V_{REF}$ or $-V_{REF}$ voltage, while the coarse discharging uses their difference, which is twice the size.

The outputs of the comparators A6 and A9 are fed to the control logic and are used to monitor the integrators during the discharging cycles.

Because the gains of A2 and A3 are parts of the transfer function of the converter and should be stable, a dynamic matching of the feedback resistors is performed [7]. This principle relies on use of resistors with equal values that are interchanged in consecutive measurement cycles and placed in all possible combinations. This way, any deviation caused by their production tolerances or temperature change is almost completely cancelled.

B. Transfer function

The conversion procedure relies on balancing of the applied charge to the integrators from the sensor capacitance and from the reference charge generators. Using the expressions for these charges, the transfer function of the converter can be derived:

$$C_X = \frac{N_X \, \Delta t}{2 \, K_A \, N_{EXC} \, G_{EXC} \, R_1} \qquad (2)$$

In the above expression, N_X is the value of the charge counter, Δt is the period of the reference frequency, K_A is the chosen ration of the coarse and fine charge generators, N_{EXC} is the number of excitation transients used for the conversion cycle and G_{EXC} is the gain of the excitation amplifier. Equation (2) demonstrates that the transfer function of the converter depends on one resistor and one time reference. These components are available in versions of very high accuracy and stability, which leads to good stability of the converter, as well.

IV. HANDLING OF CIRCUIT NON-IDEALITIES

The transfer function presented by expression (2) is derived by neglecting four major non-idealities and limitations of the components used to builds the circuit:

- Input offset voltage of the amplifiers;

- Charge injection of the analog switches;
- Limited speed of the amplifiers;
- Dielectric absorption of the integrator capacitor.

Next, we shall discuss each of the above-mentioned non-idealities and limitations, and the corresponding measures taken to minimize their negative effect on the performance of the CDC.

A. Offset voltages of the amplifiers

The offset voltage of the amplifiers is integrated along with the signal and will introduce an unacceptable error if no precautions are taken. In this respect, the critical stages of the circuit are: input amplifier A1; single-ended to differential converter A3; instrumentation amplifiers A4, A7; and integrators A5, A8. The chosen approach for minimization of this error is to keep its value constant and to split the conversion procedure into equal intermediate cycles with opposite signal polarity. In this way, the integrated offset error cancels itself in the sum of the intermediate results.

For amplifiers A1 and A3, these conditions are fulfilled if the input amplifier is connected to each of the integrator channels for equal time intervals. Provided the offset is constant, the equivalent charge error cancels itself by summing the results for the positive and negative excitation transients even in the same conversion half-cycle.

For the instrumentation amplifiers and integrators, the offset error is canceled by performing two half-cycles with the integrator channels exchanged. If the first channel is accumulating the charge from the positive excitation transients during the first half-cycle, it is accumulating the charge from the negative transients in the second half-cycle and vice versa. By keeping the duration of both half-cycles equal, the offset error cancels itself in the total result.

B. Charge injection of the analog switches

When a real analog switch is operated in the signal path, some amount of charge is transferred to its nodes and is added to the signal. This type of error can be canceled out in the same way as the offset voltage of the amplifiers, provided the number of operations for each switch is kept equal in both conversion half-cycles. This condition means that a particular switch should be operated in every half-cycle even if not needed. Because the injected charge does not depend on the duration of the switch operation, this requirement is easily fulfilled by applying an additional short pulse with fixed duration and opposite polarity each time a coarse or fine reference charge is applied.

The charge injection of the switch is a function of the voltage at its poles. For this reason, the switches in the presented solution are operated at the same voltage during the sequential conversion half-cycles, thus ensuring almost full cancelation of the error from this source.

C. Limited speed of the amplifiers

The implemented charge-balancing principle assumes zero voltage at the inverting input of the amplifiers in the input stage and in the integrators. At a high frequency, however, the performance of the operational amplifiers deteriorates and this condition cannot be met. For this reason, a low pass filter is provided in the excitation stage which rejects the high frequency components of the signal before they reach the input amplifier and integrator stages.

D. Dielectric absorption of the integrator capacitor

The dielectric of a real capacitor absorbs a part of the applied charge and releases it later. The process can be modeled by multiple RC-networks with a variety of time-constants in parallel connections [8]. The consequence is that the balancing charge applied to the integrators is a function of the charge stored not only from the current conversion, but also from the previous conversions. This results either in channel crosstalk when multiple sensors are measured simultaneously or in uncertainty in the measured value for the single channel if the capacitance of the sensor is not constant.

To minimize this effect, a PPS capacitor with low dielectric absorption is chosen for the integrator stages [9, 10]. Additionally, using multiple intermediate discharging cycles instead of one discharging cycle reduces the equivalent voltage across the capacitor, which leads to lower dielectric absorption.

V. EXPERIMENTAL RESULTS

A prototype has been built to demonstrate the advantages of the proposed solution (Fig. 3). A precision 100 kOhm 0.01% Z201 metal foil resistor from Vishay and 40 MHz CFPT-126 temperature compensated quartz oscillator from IQD are used as reference components. The power consumption of the input amplifier and the analog-to-digital converter is 45 mW and 800 mW, respectively.

The initial accuracy and temperature stability of the two prototypes was measured with a 10 pF primary standard capacitor 1404-C and an ultra-precision capacitance bridge AH2700A. Because the specified temperature stability of the standard capacitor was worse than the expected stability of the board, for each test the capacitor value was measured with the capacitance bridge and the bridge reading was taken as a reference. Both CDC prototypes were tested in a climate chamber at temperatures from 15°C to 55°C. The measured data are presented in Table 1 and in Fig. 4 and Fig. 5.

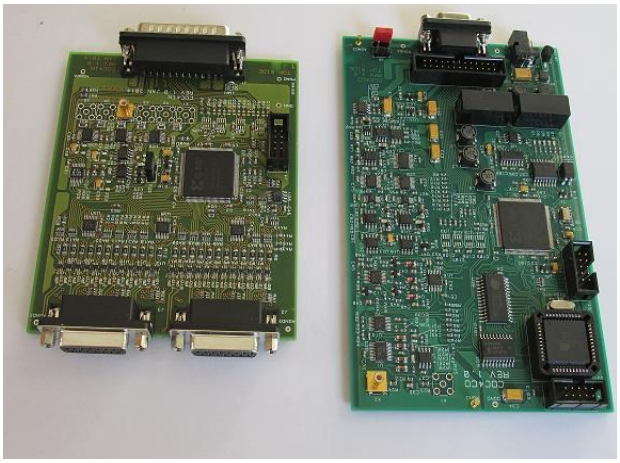

Fig. 3. Assembled boards of the input amplifier (left) and the analog-to-digital converter (right).

The prototypes were tested without any calibration or adjustment procedure. The maximal measured value of the offset capacitance is 61 aF. For 18 pF measurement range, this offset results in an offset error of just 3 ppm. As can be seen in Fig. 6, the temperature coefficient of the offset is about -1 aF/°C.

Table 1. Temperature Test Data.

Temperature (°C)	15	25	35	45	55
	Device A				
Offset error (aF)	54.8	49.0	38.9	18.6	24.5
Gain error (aF)	-351.8	-614.8	-754.1	-808.8	-849.4
RMS noise (aF)	161.7	157.4	156.9	155.9	152.3
Peak noise (aF)	539.1	498.5	498.5	518.8	539.1
	Device B				
Offset error (aF)	61.4	41.9	32.6	23.2	11.6
Gain error (aF)	-16.8	-183.4	-289.8	-334.6	-328.1
RMS noise (aF)	171.6	172.6	177.8	173.8	163.2
Peak noise (aF)	559.5	508.6	569.7	539.1	498.5

Measurement conditions: 18 pF measurement range, 2 ms conversion time, 1000 measurement samples, 10 pF standard capacitor connected to CDC with 1 m coaxial cable. The offset error is the CDC reading with all inputs disconnected. The gain error is the difference between CDC reading with offset correction and AH2700A precision bridge reading. Peak noise is the maximal deviation from the average value of all samples. RMS noise is the standard deviation of all samples for a 100 pF cable capacitance at the input.

The maximal value of the gain error is 849 aF for a 10 pF measured capacitance, resulting in 0.0085% accuracy. The tolerance of the reference resistor R1 is 0.01%, which means that both prototypes comply with the expectations for this parameter. The temperature stability of the gain is about -2 ppm/K at low temperatures and drops to almost zero at 50°C.

The RMS noise of the converter with a 100 pF cable capacitance at the input is 170 aF for an 18 pF range and 2 ms conversion time. This is equivalent to 17-bit resolution. Because the range selection of the converter is performed by changing the excitation amplifier gain, the input amplifier sensitivity and noise remain the same for

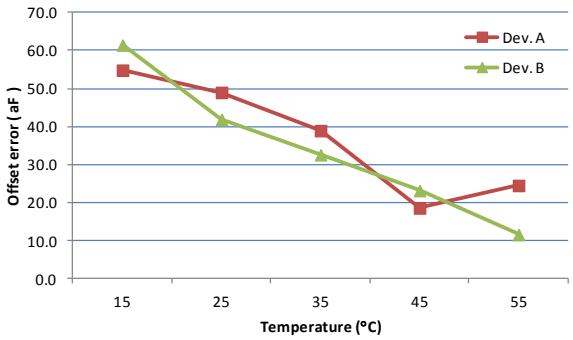

Fig. 4. Offset error as a function of temperature for an 18 pF range.

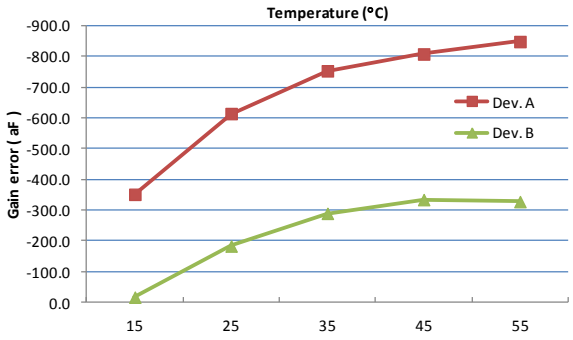

Fig. 5. Gain error as a function of temperature for an 18 pF range.

all ranges. For this reason, the CDC resolution does not depend on the measurement range.

The long term stability of the converter was tested with the continuous measurement of a 10 pF standard capacitor for 34 hours at constant temperature (Fig. 6). Both the converter and the capacitor were kept in a climate camber at 23°C. The observed capacitance variations were less than 10 aF (1 ppm). It was clearly visible in the plots that these variations were correlated with the temperature fluctuations of the chamber. For this reason it can be expected that the part of the variations caused by long term drift is lower than the measured

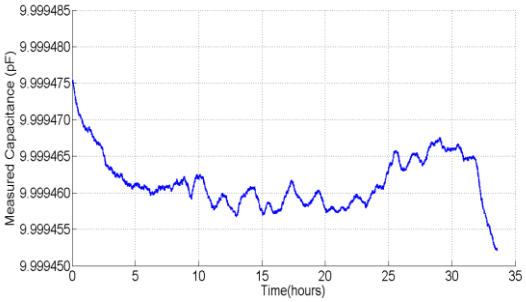

Fig. 6. Long-term stability test: 10 pF standard capacitor measured at 18 pF range.

value.

The long term stability of the offset was tested in the same experiment (Fig. 7). For the 18 pF range, an offset of 47 aF with a variation of 1 aF was observed during 34 hours of continuous measurement. This test in conjunction with the temperature stability tests

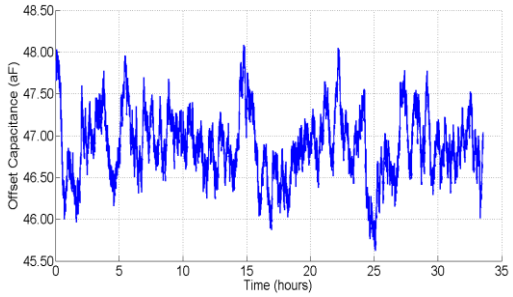

Fig. 7. Long-term stability test: offset capacitance measured at 18 pF range.

demonstrates the very good efficiency of the implemented solution for offset cancelation.

VI. CONCLUSION

The presented design for capacitive sensor interface is based on comparison of the unknown capacitance with resistance, resistance ratio and time. The respective components for these physical quantities are available in versions of very high stability. The implemented measurement procedure effectively suppresses the noise of the circuit outside of a narrow band, which results in high dynamic range of the conversion. These two conditions make the interface a promising candidate for wide range of industrial and metrological applications, where high resolution and stability are required. The experimental results prove the performance advantages of the presented solution.

VII. ACKNOWLEDGEMENT

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