NFC RF Analog Challenge and Enhanced High Speed Transmitter Design

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Abstract- This paper investigates the inherent radio frequency analog challenges associated with near field communication systems. Furthermore, the paper presents a digital based sigma-delta modulator for near field communication transmitter implementations. The proposed digital transmitter architecture is designed to best support data intensive applications requiring higher data rates and complex modulation schemes. An NFC transmitter based on a single-bit sigma-delta DAC is introduced, and then the multi-bit extension with necessary simulation results are presented to confirm the suitability of the architecture for near field communication high speed applications**.**

I. INTRODUCTION

Near Field Communication (NFC) is a wireless data interface technology specified at 13.56MHz. Data transfer between NFC devices is achieved using alternating magnetic fields within the operating volume. In addition to supporting existing Bluetooth and Wi-Fi technologies, another popular NFC application so far has been in mobile phones, for information transfer and making payments. However, NFC has several other applications such as e-passport, ticketing, healthcare and multimedia to mention a few. To implement applications requiring bulk data, further development is required to both NFC standards and NFC enabled devices which are limited by the current NFC highest data rate specifications of 848kbit/s [1]-[2]. Witschnig and Merlin discuss the current specified data rate limitations and propose enhancing the data rate of NFC systems by increasing the symbol rate to 3.39Msps achieved through using 16 PSK modulation. This would allow the bit rate to increase to 13.56Mbps [3].

This study tackles this issue by proposing techniques for developing NFC devices to support higher data rate applications by introducing a digital sigma-delta (Σ-Δ) modulator in the transmitter design. The organization of this paper is as follows: Section II presents the fundamental operation and challenges of NFC systems. A single-bit Σ-Δ transmitter concept is introduced in Section III. A discussion of the state-of-the-art multi-bit NFC transmitter is given in Section IV. The findings of this work are summarized in Section V.

II. FUNDAMENTAL OPERATION AND CHALLENGES OF NFC SYSTEMS AT 13.56 MHZ

NFC technology is based on the magnetic coupling between devices as shown in the block diagram of the reader and tag in Figure 1. The magnetic field generated by the initiator is directly proportional to the current flowing through an inductive antenna element at a fixed carrier frequency of 13.56MHz. The generated field is used as a carrier for modulated signals and a means of conveying energy to power a tag when necessary.

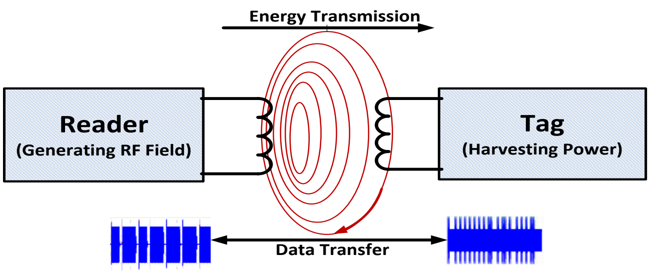

Figure 1: Block diagram illustrating a basic NFC system

An NFC system should be able to operate both as a reader and a tag. NFC devices can operate in several modes including tag emulation mode, reader mode and Peer-to-Peer (P2P) mode. When the device is taking on a role of an interrogator, then it is operating as a reader. This mode facilitates NFC enabled devices to read and write data to NFC enabled tags. In tag emulation, the device may operate in either passive mode or active mode. In the passive mode, the device harvests its power from the magnetic field provided by the initiator, hence requiring the reader to be designed to provide enough power. Conversely, active mode operation requires the tag to provide its own power. In the tag emulation mode, the NFC device emulates a contactless card and thus can be used for applications such as payments and ticketing. Finally, the NFC P2P mode is communication between two devices working in active mode and is used to transfer data such as photos between 2 NFC enabled devices [4].

The RF challenges arise when two NFC devices interact in the magnetic field within a specified operating volume. When a tag is introduced in the reader's magnetic field, it presents a load determined by its antenna system configuration. As a result, the tag introduces changes to the reader impedance with variations in the coupling factor

ISBN-10: 84-616-5438-2 | ISBN-13: 978-84-616-5438-3

(*k*), as it moves within the reader's magnetic field. In a real device, this would result in a reduced reader antenna input voltage, ultimately causing a drop in the reader's magnetic field strength. Consequently, when communicating with passive tags, the power harvested by the tag from the field drops and may become insufficient to power the tag. Figure 2 shows the results of a lab test investigation using an NFC enabled device and testing according to the NFC forum's power transfer specification. The distances indicate the antenna alignment of the 2 devices used in the test. Further details of this test are outlined in the NFC Forum analog specification [5]. The results in Figure 2 show voltage drops around the antenna position *X*=0, *Y*=0, *Z*=0, which then increase significantly as the device antennas are offset. However, when the antennas are offset further, the voltages decrease again. The variations in voltage confirm the NFC's inherent coupling effect, which is a vital consideration in NFC transmitter design.

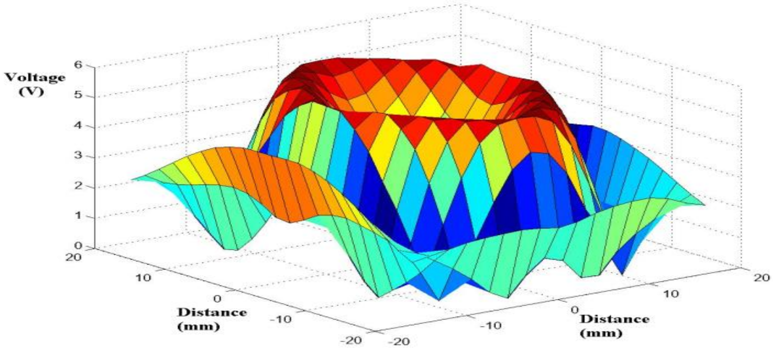

Figure 2: A graph of voltages seen in the field of the NFC enabled device.

The design process, takes into consideration the NFC's inherent challenges to design a transmit system that is easy to implement and efficient when operating with passive tags as well as in P2P mode. This coupled with the need to support future applications requiring higher data rates, clever transmitter design to maintain small chip area as well as low current consumption without compromising performance. The next section presents a Σ-Δ based digital transmitter design with a view to enhancing NFC device performance.

The NFC transmitter architectures proposed so far are analog-based. Porting such designs to a different technology is difficult. Furthermore, some of the proposed architectures employ a Delay Locked Loop (DLL) which relay on the matching of analog components, which may introduce inaccuracies in the data stream modulation. In addition, the DLL need to be locked before the transmitter can be used [6]. This paper introduces a compact digital based transmitter to reduce chip area depending on the technology of implementation (the smaller the geometry, the more area saving), facilitate design porting with changes in the technology and further supports higher order modulation schemes which are required for higher data rates.

III. SINGLE-BIT SIGMA DELTA MODULATOR CONCEPT

The approach undertaken in this study is to simplify an NFC transmitter design by using a digital direct drive technique. The aim is to design a transmitter that can satisfy the current NFC specifications and further support data intensive applications requiring higher order data modulations, such as in applications where firmware transfer to a new phone or simply phone firmware updates are undertaken through the NFC interface. The block diagram of the proposed architecture is depicted in Figure 3. In this architecture, an NFC co-existence filter is included as a requirement for the antenna system to help lower signal degradation. This will be studied and shown to be the case through simulation in Section IV. Two half-drivers allowing a full-bridge configuration to drive the co-existence filter are fed directly from the Σ-Δ modulator. The half-drivers are mainly large Complementary Metal Oxide Semiconductor (CMOS) inverters and are driven by a digital band-pass Σ-Δ modulator.

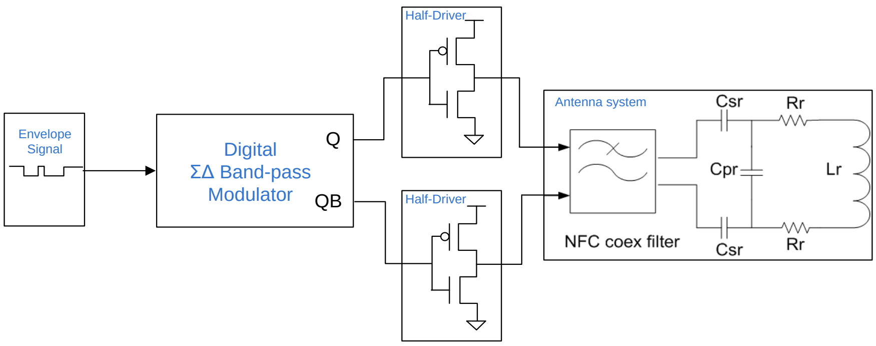

Figure 3: Block diagram of proposed single-bit transmitter architecture

In order to get a system centered at 13.56 MHz, the sampling frequency f_S of the modulator is chosen to be four times the center frequency, hence f_S = 54.24MHz. Currently, the NFC standard uses Amplitude-Shift-Keying (ASK) modulation with a maximum data rate of 848Kbps. From the theory of amplitude modulation, the bandwidth occupied by this signal can be calculated to be 2*848 kHz, which is 1.7MHz. This means that the Over Sampling Ratio (OSR) of the system is OSR = f_S /(2* f_B) = 16. In order to derive a band-pass Σ-Δ modulator from its low-pass counterpart, the pseudo *N*-path transformation with *N*=2 is employed. One of the consequences of this transformation is spectrum compression in the band of interest. This means that if the low-pass version is designed to achieve a Signal-to-Noise Ratio (SNR) over a bandwidth BW, the band-pass equivalent will provide the same SNR for a given center frequency (i.e. 13.56 MHz in this case) as long as it has the same bandwidth. The key parameter used to evaluate the proposed architecture is the SNR, which needs to be large enough to support higher-order modulation. For that reason, the target peak SNR is 60 dB. In order to measure the SNR, a Continuous Wave (CW) tone will be injected into the system and the Single Sided SNR (SS SNR) will be measured. In the case of an ASK modulation, the Dual Sided SNR (DS SNR) is the same as that of the SSB SNR. Schreier's toolbox is used in this design process [7]. The Noise Transfer Function (NTF) of the proposed low-pass Σ-Δ modulator is hence found and presented in (1).

$$\mathrm{NTF(LP)} = \frac{(z-1)(z^2-1.9770z+1)}{(z-0.6657)(z^2-1.5400z+0.6599)} \tag{1}$$

Using the pseudo *N*-path transformation with N = 2 and replacing z with $-z^2$, the low-pass implementation is transformed into its band-pass equivalent with a center frequency of 13.56MHz. The band-pass NTF obtained via the pseudo 2-path transformation is given in (2).

$$\mathrm{NTF(BP)} = \frac{(z^2+1)(z^2-0.1517z+1)(z^2+0.1517z+1)}{(z^2+0.6657)(z^2-0.2910z+0.8123)(z^2+0.2910z+0.8123)} \tag{2}$$

Figure 4 shows the block diagram of the band-pass Σ-Δ modulator. The system includes a digital mixer, a single-bit quantizer and a digital band-pass filter. The digital envelope signal is first up-converted to a 13.56 MHz frequency before feeding it to the band-pass Σ-Δ modulator. In order to add the 13.56 MHz carrier, a Direct Current (DC) signal has to be injected in front of the digital mixer. This DC level can be set as required, but has a maximum limit of 0.7*Vdd to ensure that the Σ-Δ modulator is not overloaded. Each Σ-Δ modulator stage uses a resonator, whose transfer function is given in (3). The single-bit quantizer outputs +1 or -1, which depends on the polarity of the output signal of the third resonator. The differential output of the modulator is then fed to the large CMOS inverters to drive the NFC antenna as was shown earlier in Figure 3.

$$H_{BP}(z) = \frac{-z^{-2}}{1+z^{-2}} \tag{3}$$

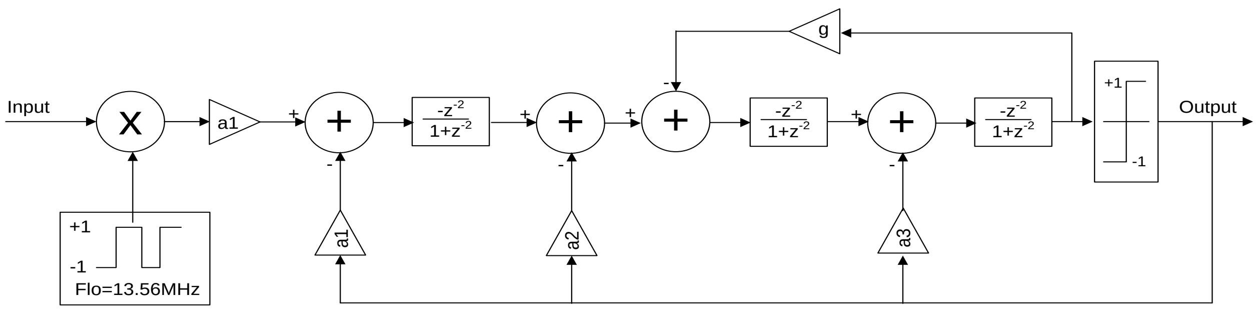

Figure 4: Block diagram of the band-pass modulator

Current specified NFC ASK modulation schemes range from 10% to 100% depending on the technology (NFC-A, NFC-B and NFC-F) [2]-[5]. To demonstrate the performance of the system, an NFC ASK signal with a modulation index of 100% is applied at the input. The corresponding output spectrum of this system is shown in Figure 5. The system SNR is calculated by taking the ratio of the power of one modulation side band (in red) over the power of the noise (in green) integrated over half of the bandwidth. The results in Figure 5 achieve an SNR of 42dB, which is below the target 60dB required for higher-order data modulation schemes. On the other hand, to accurately demodulate an ASK signal in the current NFC specification, a minimum SNR of 15 dB is required to achieve the bit error rate of less than 10e-3. From the given results, the margin provided by this digital transmitter is enough for 100% ASK. However, if the modulation index is reduced to 3.5% ASK, the system is limited in that the SNR is decreased below 15dB. Furthermore, there are possible analog degradations in the system which can compromise performance. One example of degradation is the non-linearity generated by the CMOS drivers (cross-over distortion), which requires the design to have accurate rise and fall times to avoid further degradation to the SNR.

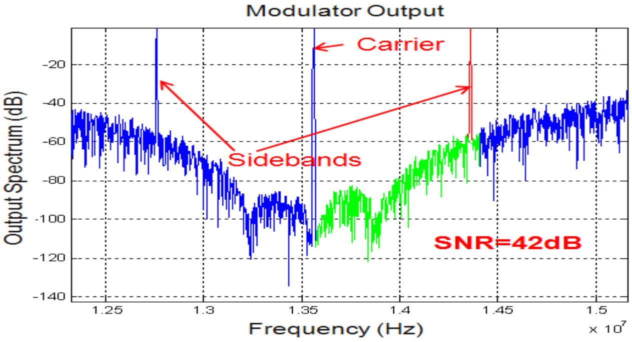

Figure 5: Modulator output spectrum of a 100% ASK signal

To further check the performance of the single-bit transmitter, the Σ-Δ modulator output spectrum was investigated for the severity of the out-of-band spectral emissions (transmit emissions) as limited by the emission regulating organizations. Figure 6 shows the simulation results of the output spectrum of the Σ-Δ modulator when driving it with an NFC signal. The spectrum exhibits tones, which might compromise emission levels. This is compounded by the fact that the system is using only a 1-bit quantizer to represent the information, which results in a large amount of noise being introduced over a larger bandwidth. The coexistence filter and the antenna system help attenuate this noise. A better solution, however, involves the design of a multi-bit Σ-Δ modulator which certainly improves the performance of the system regarding the SNR and further reduce the transmit emissions.

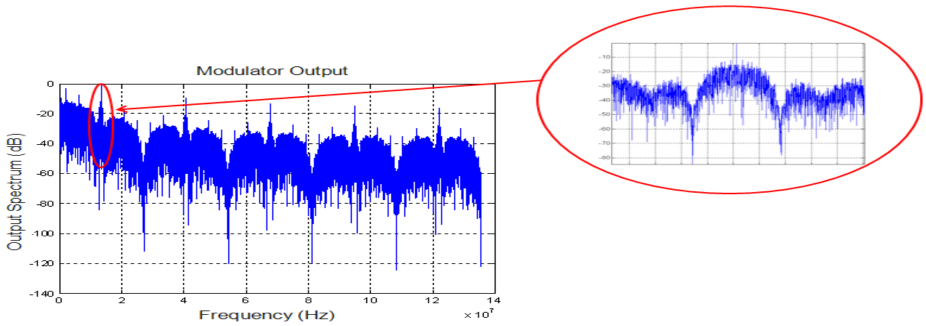

Figure 6: Transmit emissions for a mono-bit modulator

IV. MULT-BIT SIGMA DELTA MODULATOR

To improve the SNR of the transmitter and minimize the out-of-band emission, a multi-bit Σ-Δ modulator is used as shown in Figure 7. An optimization was performed to achieve a suitable solution with the lowest modulator order and the minimum number of quantizer bits. This is achieved by varying the modulator order or the quantizer bits. Considering that the modulator is digital, the NTF can be shaped more aggressively by pushing more quantization noise to higher frequencies as there are no analog impairments that could degrade the stability of the system.

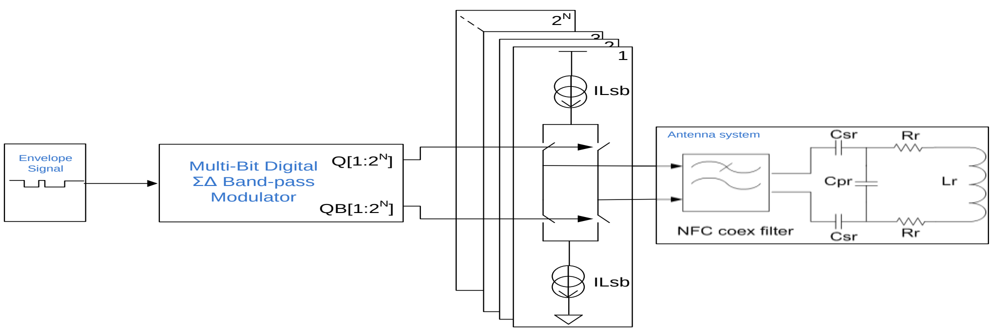

Figure 7: Block diagram of proposed multi-bit transmitter architecture

A third-order Σ-Δ modulator was found to provide the best trade-off regarding complexity, peak SNR and dynamic range. A second fine tuning procedure was aimed at choosing the number of bits for the quantizer (N_q). Figure 8 presents the results of this process. For implementation simplicity, N_q = 1 would be the preferred solution. However, Figure 8 reveals that the minimum required N_q to achieve the targeted performance is 3. On the other hand, Figure 8 confirms that a single-bit solution satisfies the currently specified NFC modulation schemes. The final solution utilizes a 3-bit based Σ-Δ modulator which drives a set of 8 differential current sources into the co-existence circuit connected to the antenna. Using the same optimization process as the single-bit transmitter, the 3-bit low-pass Σ-Δ modulator is designed. The use of a multi-bit based Σ-Δ modulator allows to push Lee criterion [7] by using the maximum gain of the NTF over all frequencies (NTF (∞)) = 5, hence deriving a NTF with a more aggressive noise shaping. Once more, the pseudo *N*-path (*N* = 2) transformation was used to translate a low-pass topology to its band-pass counterpart. The output spectrum of the multi-bit Σ-Δ modulator, which is tested with a 100% ASK signal, is presented in Figure 9.

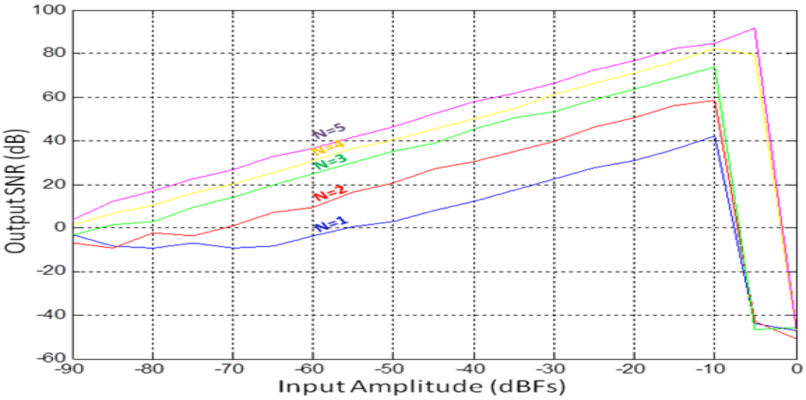

Figure 8: SNR versus Input Amplitude Sweeps for different number of bits in the quantizer

Figure 9 demonstrates that the system can achieve an SNR of 72.5dB, which is an improvement of 30.5dB compared to the single-bit version. The increase in SNR can be attributed to the improved noise-shaping performance and multi-bit quantizer. To reach the minimum 15dB SNR requirements in order to achieve a demodulation with a bit error rate less than 10e-3, the modulation index has to be reduced to 0.1% ASK, which is much lower compared to the 10% ASK currently specified.

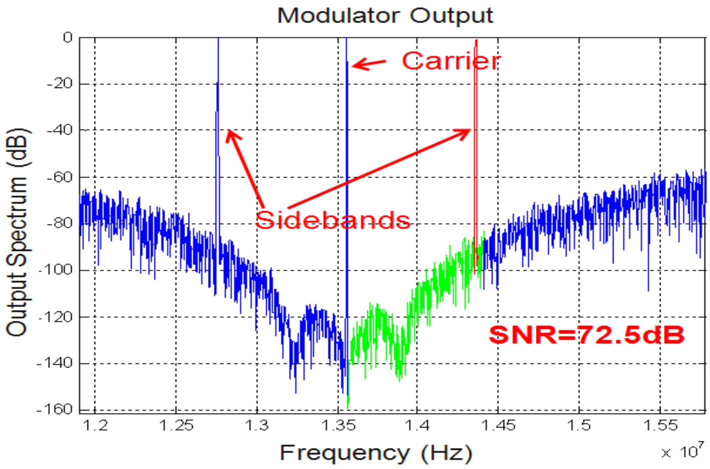

Figure 9: 4-bit modulator output spectrum with 100% ASK signal

Employing the multi-bit version improves the resolution of the system allowing this architecture to be used with higher-order amplitude modulation as well as high-order phase modulation schemes. This radically increases the data rate of the NFC communication to above the standardized 848kb/s. Furthermore, this architecture should distinctly improve the out-of-band emissions. To verify the reduction, an ASK NFC signal with 100% modulation index is injected into the system and the results are presented in Figure 10. Comparing the results for the single-bit counterpart of Figure 6 and those of the 3-bit architecture in Figure 10, the reduction in the tones across the spectrum is evident.

In implementation, one of the main drawbacks of the multi-bit version will be the non-linearity produced by the mismatch between the different current sources. A way to mitigate this issue would be to employ dynamic element matching to shape the mismatch of those unit current sources. Since the current sources need headroom to accurately deliver their current to the load, the efficiency of the multi-bit version is expected to be lower than the single-bit one. An improvement would be to create a zero current state for each current source to avoid injecting current in the antenna when it is not required. The study of the coexistence filter and antenna combination shows that it is more suited to drive the antenna system with a current instead of a voltage source. A simulation in the Cadence spectre environment shows the benefits of a coexistence filter driving the antenna. Figure 11 shows the circuit and results of the antenna system with and without the co-existence filter.

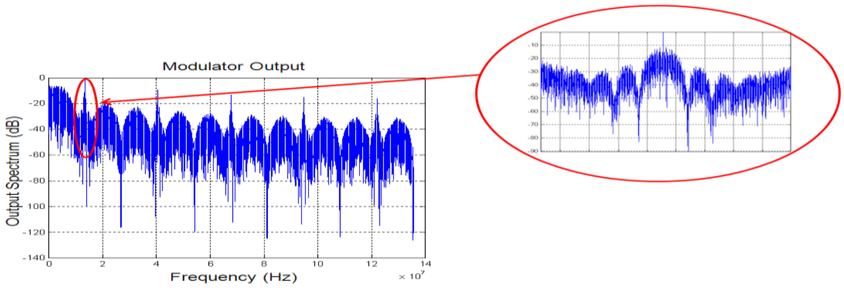

Figure 10: Transmit emissions spectrum of a 3-bit modulator

The results reveal that to drive 100mA to energize a tag, a voltage in excess of 14V is required between Tx1 and Tx2 making IC implementation difficult. Adding a co-existence filter attenuates the high frequencies and provides an impedance transformation resulting in lowering the impedance presented between Tx1 and Tx2. Figure 11 shows that the voltage required to drive 100mA is reduced to 3.86V, which is more reasonable and has the potential to be reduced further. A voltage of 3.86V with a current of 100mA is equivalent to a 38.6 Ω resistance. Such a low input resistance suggests that a current drive is more appropriate, which fits the proposed multi-bit architecture.

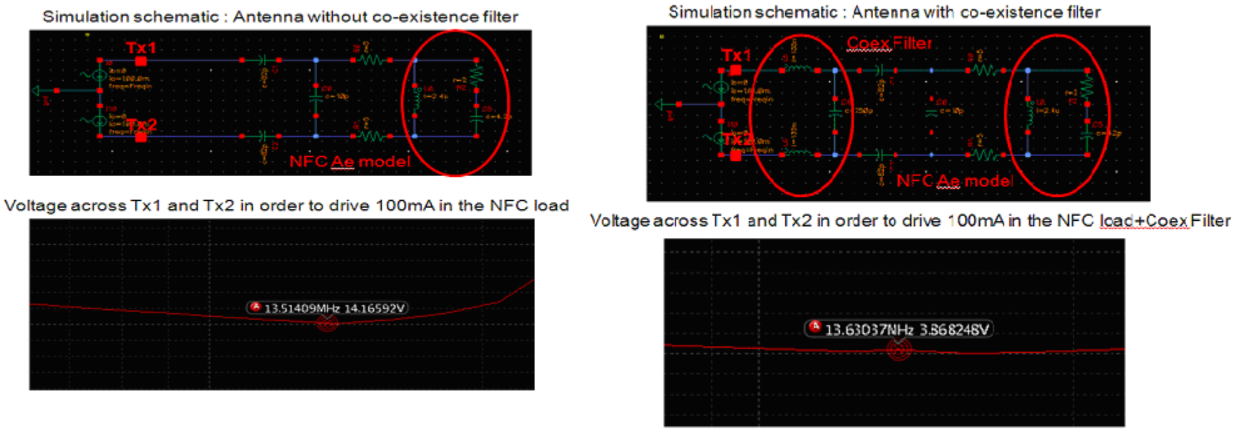

Figure 11: Simulation of the NFC antenna with and without the co-existence filter

V. CONCLUSION

This paper has presented an easily implementable, digital transmit architecture that can support both current NFC applications as well as probable future applications. The current NFC standards limit the wider adoption of NFC for certain applications such as firmware updates on mobile devices, hence the paper has presented a transmit architecture that demonstrates the possibilities of extending applications that would require higher-order modulation schemes to encourage development in that direction. The paper outlines the design of a Σ-Δ modulator based transmitter using a single-bit quantizer. This was then extended to a 3-bit quantizer based Σ-Δ modulator. Simulation results have shown that the single-bit based transmitters achieve a SNR of 42dB with 100% ASK, which then drops to 15dB with 3.5% ASK. As a result of this modulation index reduction, a 3-bit architecture was deemed more appropriate. The SNR was increased to 72.5dB and performed within the recommended SNR range with 0.1% ASK. A further noticeable benefit was reduced transmit out-of-band spectral emissions. To further enhance the performance, the co-existence filter was placed before the antenna. This decreased the antenna voltage requirements from 14V to 3.68V, reducing the input resistance requirements. This was found through simulation to work best with the current drive based multi-bit architecture presented in this paper.

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