Performance comparison between traditional and RNS-based ADC.

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Abstract.

Recently a new architecture for an analog to Residue Number System converter was proposed by the authors [1]. In this paper a comparison of the performances, in terms of probability of LSB error due to internal noise, between a traditional ADC converter and this said analog to RNS converter is given.

Keywords:
ADC, RNS, error self-correction

1. Introduction

Residue Number System (RNS) arithmetic has received great attention in the literature [2] and its advantages in performing complex calculations have been clearly pointed out. These advantages are mainly: absence of internal overflow, absence of internal rounding errors, parallelization of the calculations, reduced size of processors with respect to the traditional ones maintaining the same dynamical range, reduced power consumption, possibility of low redundancy for detect and correct failures. Despite these concrete advantages, practical applications are until now very poor, mainly for the complex conversion from binary to RNS and viceversa. So a direct conversion from analog to RNS representation becomes very attractive. However, a direct conversion from analog to RNS representation (ARNS in the following) appears very difficult to implement, particularly by the fact that the conversion errors, being the final representation a non-positional one, can induce macroscopic errors. Particular procedures for this conversion have been proposed in order to avoid these errors [3]. These techniques are essentially based on particular type of folding and on modulus redundancy in order to control the correctness of the results.

This paper is focused on the internal noise of the A/D converter (ADC). We suppose that the effect of this noise **affects only the LSB** of the digital representation. To improve the correctness of the converter output, we can perform many conversions of the same quantity and then assume as correct result that selected on the basis of the majority voting rule. However, the implementation of this methodology using a single ADC produces an operating speed too slow. On the other hand, conversion architectures having some ADCs working in parallel become too complex.

Recently, in order to take advantage from the RNS representation in the internal processing of the Virtual Instrument (VI), a new architecture for a RNS flash ADC was proposed by the authors [3]. This architecture, which exhibits a complexity comparable with that of a traditional ADC, provides a suitable algorithm for the detection and the correction of the RNS residues, avoiding the catastrophic errors that can be induced in such a non-positional representation.

x

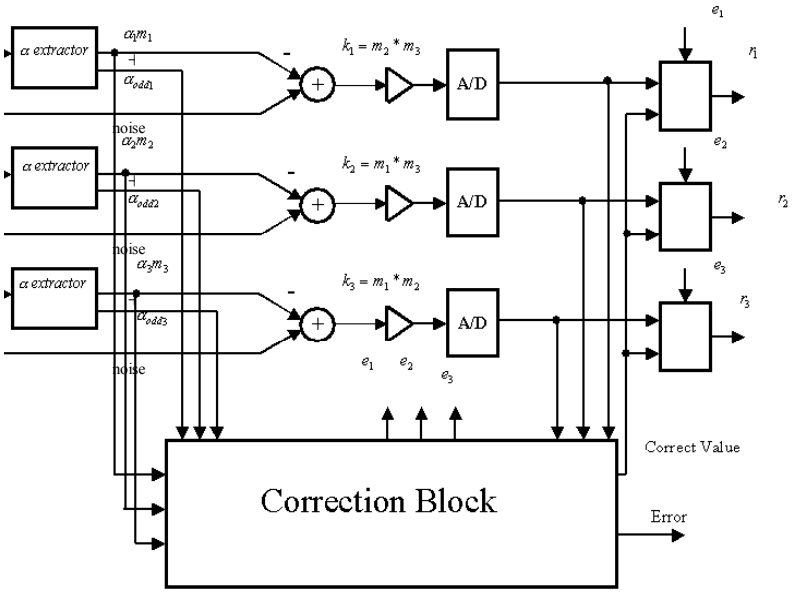

Fig. 1 Architecture of the ARNS converter which is compared with a traditional ADC.

We show in this paper that the correction of the residues, which is introduced as said above to avoid catastrophic errors, results in a reduction of the effects of internal noise of the analog to residue converter that exhibits now a robustness with respect to noise better than a traditional ADC.

In the following section 2 we briefly describe the correction algorithm. In section 3 the evaluation of the overall noise of the RNS converter is compared with the same noise supposed in a traditional ADC. In section 4 some results of simulation are compared with the calculated ones and concluding remarks are presented.

2. Description of the architecture

A RNS is based on N pairwise prime moduli m_i , i=1,...,N and can represent univocally M = $\prod m_i$ different numbers. The representation is obtained through **N** residual quantities $\mathbf{r_i}$, **i= 1,…,N**. Consequently, an integer **X < M** is represented by

$$\mathbf{r_i = <X>_{mi} = <\alpha m_i + r_i>_{mi} , i =1,\ldots,N} \qquad \mathbf{(1)}$$

We suppose, as in most cases, that all the moduli m_i are odd. In this case, starting from the last right side of (1), we can remark the following properties:

i - $\alpha_i m_i$, being m_i an odd number, is odd or even according to α_i;

ii – if we consider the quantities **X,** α_i **,** $\mathbf{r_i}$ in binary form

$$\mathbf{LSB(X)=LSB[LSB(\alpha_i) + LSB(r_i)] = p_i \quad i=1,\ldots,N} \qquad \mathbf{(2)}$$

with $\mathbf{p_i \in \{0,1\}}$ and **LSB (X) = , i = 1,…,N** (in a correct conversion, all the p_i's must be equal to each other and the set of r_I represents in RNS the correct value of the input).

In absence of noise, we can evaluate the residues by using separate analog to residue converters which was proposed in [3] as two stage (an analog and a digital ones) flash converters. The obtained RNS representation corresponds to a binary quantity that differs from to the analog input of a quantity less than (ARNSC in the following) the quantization step used. In other words, in absence of noise, the behavior of the analog to

RNS converter is similar to that of a traditional ADC.

Now we suppose that, due to the internal noise of the converter, some errors are introduced in the ARNS conversion (introducing, as said above, catastrophic errors). In this case some of the said p_i are not equal to the others. We can assume that the correct value of the $\mathbf{p_i}$'s $(\mathbf{p}^*)$ can be chosen on the basis of the majority voting rule. So we can isolate the wrong parities $\mathbf{p_j}$ **, j =1,…,L** and correct the related residues. An example of architecture implementing the whole ARNS converter and the correction said above was given in [3] and is sketched in Fig. 1. This correction, introduced to avoid macroscopic errors, as said above, gives to the ARNS converter that we are considering a better accuracy than a traditional ADC, as will be shown in the following, firstly by calculation and then by simulation.

For the sake of an effective comparison, the internal noise of the converter of each residue is considered as an input noise, as shown in the Fig. 2, having a gaussian distribution. The presence of this noise can induce some errors. However, due to the action of the correction block, in the presented case of only three moduli, if one of the three residues is wrong, on the basis of the majority voting rule, as described in [1], this wrong residue can be corrected in such a way that the RNS representation becomes again correct.

3. Error evaluation

The structure of the proposed ARNS converter is shown in Fig. 1. N ideal converter chains (one for each modulus) compose that scheme. Each chain is considered ideal; i.e. noise and non-linearity effects are absent. Moreover, the overall actual internal noise is taken into account by external noise sources placed at the input of each modular converter. In the following analysis, we consider truncation quantization but similar methods can be developed for analyzing ARNS converters based on other quantization laws.

Let us consider an input noiseless voltage V and the chain conversion related to the i-th modulus. The sum of the input and the noise voltages gives the final value $V_i = V + n_i$, where n_i represents the introduced noise.

It is worth noting that, in the analog to RNS conversion, all the modular converters use the same quantization step q, therefore the distance Δ of the voltage V from the quantized quantity V' -defined by the expression $V' \le V < V' + q$ - is the same for all the modular chains. This concept is sketched in Fig. 2 where the input voltage V and its quantized representation V' are shown, together with noiseless quantization error Δ. For each modular chain is also reported the corresponding residue value x_i. In that figure, beside the quantization grid, for each modulus, is also represented the Probability Distribution Function (pdf) of the actual input voltage V_i of each channel. For sake of simplicity, our analysis supposes that all the channel noise sources have the same variance σ^2.

For the i-th modulus we have the error probability expression

$$p_e^{(i)} = \frac{1}{\sigma\sqrt{2\pi}}\left(\int_{|\Delta|}^{\infty} e^{-\frac{\varepsilon}{2\sigma}} d\varepsilon + \int_{q-|\Delta|}^{\infty} e^{-\frac{\varepsilon}{2\sigma}} d\varepsilon\right) \tag{3}$$

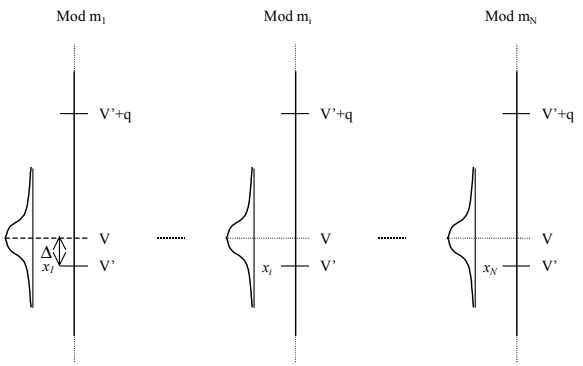

Fig. 2 Quantization voltage levels grid for the different modular chains.

Expression (3) computes the probability of obtaining a voltage value V_i lying outside the correct quantization interval. For an *N*-moduli converter, according to the majority voting rule, we are able to correct the final values of the residues $\mathbf{r_i}$ if and only if the number of wrong

residues is less than $\left\lfloor \frac{N}{2} \right\rfloor$ (here we assume that the probability of uncorrectable errors that preserve the parity (2) is negligible).
Considering all the possible correctable error combinations and their own probabilities, the probability p_c to obtain a correct conversion result is given by the following expression (4):

$$p_c = \sum_{j=0}^{\lfloor N/2 \rfloor} \frac{N \cdot (N-1) \cdots (N-j+1)}{j!} p_e^j (1-p_e)^{N-j} \quad (4)$$

The probability values of correct conversion result computed for various values of N (the number of the moduli used in the RNS representation) are compared with the probability of correct result for the traditional ADC having the same quantization step (see fig.3).
The probability curves are calculated versus the ratio σ/q. We can note that the ARNS gives better results if compared with the conventional ADC, that uses only one converter chain and whose error probability is directly given by (3).
Moreover, the performance of the self-correcting analog to RNS converter improves if the number of moduli (*N*) increases.

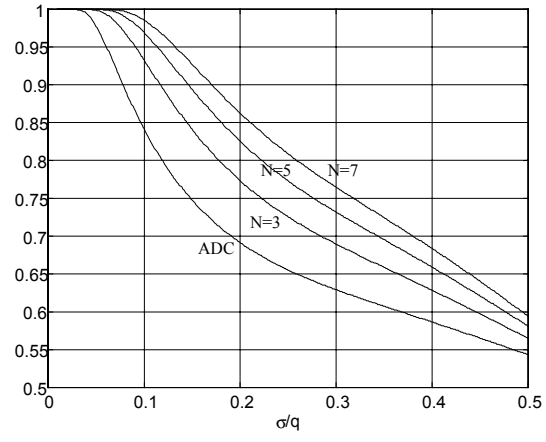

Figure 3 Probability of correct conversion for the conventional ADC and ARNS with N= 3, 5, 7 moduli.

4. Conclusions

It was observed that the majority voting rule applied to a set of conversions of the same quantity could reduce the effects of the internal noise of the analog to digital converter. This procedure, is very expensive if obtained by using a set of parallel traditional ADC's. On the other hand, if a single converter is employed, thia said procedure becomes inadequate for many different reasons. I. e. is too slow and the the conversions would happen at different instant of time.
A direct analog to RNS converter, having complexity comparable to a traditional ADC was recently proposed by the authors. This last device, in order to obtain the RNS representation of the input needs of a set of parallel modular converters having the same input. The majority voting rule is applied to these modular conversions to assure the coherence of the RNS.
It was shown in this paper that the parallel procedure applied in this said RNS converter reduces the effect of the converter internal noise. So a consistent advantage is obtained with respect to a traditional ADC. In addition, the RNS representation obtained allows the advantages proper of this said arithmetic in further processing of the converted quantities.

References

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