An analog approach to compensate for OpAmp offset and finite gain in SC circuitry: A case study of a cyclic RSD ADC

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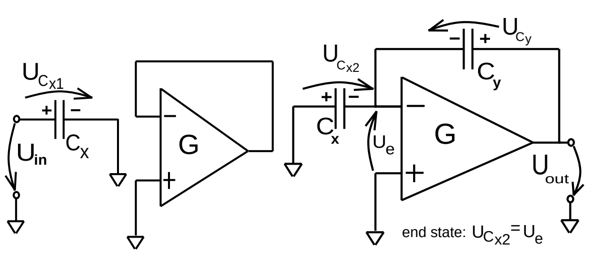
Abstract: Design of high-resolution Nyquist rate A/D converter necessitates the usage of advanced circuit techniques to compensate for arising analog errors. In switched capacitor ADC, besides the well know techniques such as bottom plate sampling, mismatch-independent and redundant (RSD: 1.5bit/stage) conversion for the elimination of charge injection, capacitor mismatch, comparator and offset sensitivity, respectively, the most utilised circuit techniques are those for OpAmp's offset and finite gain errors cancellation. An alternative technique for compensation of the errors due to finite gain and offset of Opamp in SC circuits is proposed. This novel method features a charge addition and is compared to so far used approaches based on voltage addition [1],[2]. The concept and the results of a 5V CMOS implementation of cyclic RSD ADC with ratio-independent SC technique using this correction method are discussed.

Key words: cyclic/algorithmic analog-digital converter, switched capacitor circuit, amplifier's finite gain and offset.

Introduction.

The most crucial design task of cyclic (algorithmic) and pipeline A/D converters (ADC) is the realization of an accurate multiplication by a factor of 2 for every bit cycle (loop gain = 2) or between every pipeline stage (inter-stage gain = 2), respectively, to complete the straight-forward division algorithm after each bit comparison [3]. The capacitance mismatch problem in switched-capacitor (SC) realizations can be avoided by the well known capacitance ratio-independent SC technique, e.g. [1]. However, the finite gain of an operational amplifier in every SC circuitry pushes the overall loop gain below the accurate value. In the case of a loop gain slightly lower than 2 (e.g. 1.95) an often used approach is digital calibration. Recently, [1],[2] introduced an effective approach of analog compensation for OpAmp-caused errors, the offset and the finite gain (G). The approach is based on sensing these errors in terms of voltage difference at the Op-Amp input and subsequently compensating the error by a voltage addition at the OpAmp input. We propose a different principle whereas the correction is performed by adding a charge amount (charge addition compensation), which allows a more precise adjustment of error cancellation.



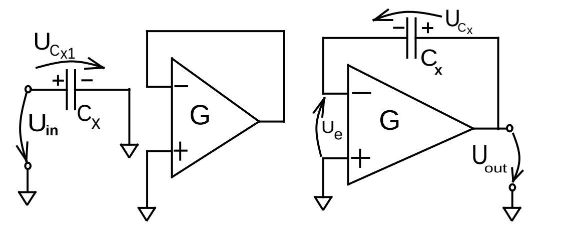
a) sample phase **b)** charge transfer hold phase

Fig.1: Origin of SC errors due to OpAmp's finite gain.

In a settled state, the impact of OpAmp's offset and finite gain cause a loss sustained charge transfer from the sampling (C_x) to the integration (C_y) capacitor. This effect is caused by a remaining non-zero differential voltage at the input ($U_e = U_{out} / G$), thus some charge remains on C_x in the hold phase (Fig. 1b). Additionally, the same voltage U_e raises another error. The voltage which appears at the OpAmp's output is not the full voltage over the integration capacitance C_y, but is reduced by U_e. Both errors together can be ascertained from the charge balance equation (1) in the case of a charge transfer between C_x and C_y (Fig.1):

$$U_{out} = (U_{in} - U_e).\frac{C_x}{C_y} - U_e = \\ = U_{in}.\frac{C_x}{C_y} - U_e\left(1 + \frac{C_x}{C_y}\right) \qquad (1)$$

Given that $C_x = C_y$ (integrator with gain = 1), the error amounts to $2.U_e$, which can be compensated for by means of an auxiliary charge $Q_k = 2.U_e.C_x$ (2)



a) sample phase **b)** C_x-reconnecting hold phase

Fig.2: OpAmp's finite gain error in a ratio-independent sample-and-hold (S&H) switched capacitor circuit.

In the case of a ratio-independent SC S&H circuit with just a single C_x capacitor being reconnected into the feedback (Fig.2), the error share coming from non-ideal charge transfer does not arise. The only remaining error is due to the U_e-reduced output voltage

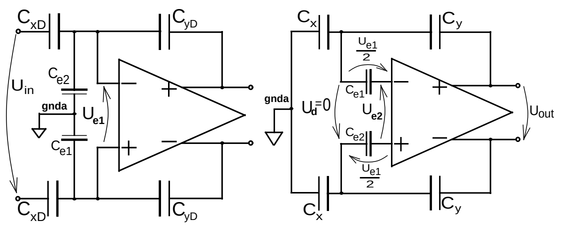
$$U_{outSH} = U_{Cx} - U_e = U_{in} - U_e \qquad (3)$$

which can be compensated for by half the charge amount compared to (2): $Q_{kSH} = U_e \cdot C_x$. Mostly, the SC correction is based on error-sensing capacitors ($C_e \approx C_x$), which will, however, withdraw from the working capacitors a charge similar to the error which impedes a true correction. Therefore, common to all correction principles the error (U_{e1}) must be determined in an earlier "predictive" phase, which simulates the actual load conditions using dummy capacitors (C_{xD} ,C_{yD}). The measured voltage U_{e1} is being used in the subsequent integration phase for the U_{e2}-error compensation. Despite of similar feedback circuitry in both phases, but due to additional prediction phase' loading by C_e the error voltage U_{e2} is non-significantly larger than U_{e1}:

$$U_{e2} = U_{e1}.(1+\varepsilon) \quad \text{with} \quad \varepsilon = \frac{\sum C_e}{C_y}.\frac{1}{G} << 1 \qquad (4)$$

Correction by voltage addition.

The correction approach in [1],[2] is likewise suitable for sampling (Fig.2) as well as for charge transfer SC integration (Fig.1). The error voltage stored on the C_e-capacitors is being reconnected serially and polarity-inversely into the OpAmp's input paths and the error this way compensated. New virtual ground nodes with $U_d = (U_{e2} - U_{e1}) \approx 0$ arise (see Fig. 3b). This way the whole charge from C_x can be transferred into C_y and at the same time the complete voltage drop over C_y occurs at the OpAmp's output without any loss. The value of sensing C_e does not have any arithmetical influence on the correction algorithm.



a) error measure phase **b)** compensation phase

Fig.3: Voltage addition based SC error compensation.

Correction by charge addition.

In the innovative charge addition based correction the value of C_e is essential. This principle is particularly suited for fully differential circuitry and so will be explained here. During the predictive phase, both measuring capacitors $C_{e1} = C_{e2}$ will be charged in shunt (Fig. 4a) up to the full differential voltage at the OpAmp's input:

$$Q_e = U_{e1}.(C_{e1} + C_{e2}) = 2.U_{e1}.C_e \qquad (5)$$

In the correction phase every C_e will be reconnected between the OpAmp's input and the analog ground (midpoint potential V_{cm}), as shown in Fig. 4b. In the initial moments of this phase, due to the parallel-serial switching of C_e capacitors a voltage doubling at the OpAmp's inputs arises ($2U_{e1}$). However, in the stable state OpAmp's input differential voltage settles to a value of U_{e2}, impressed by amplifier's degenerative feedback and the finite gain G. Thereby half of the charge $2.U_{e1}.C_e$ calculated in (5) is being transferred to both integration capacitors C_y, which compensates the error. The exact calculation of the correction charge Q_k transferred into C_y in the case of $C_{e1} = C_{e2} = C_e$ follows

$$Q_k = 2 \cdot C_e \cdot \left(U_{e1} - \tfrac{1}{2}U_{e2}\right) \qquad (6)$$

This charge increases the voltage drop U_{Cy} additionally by a value

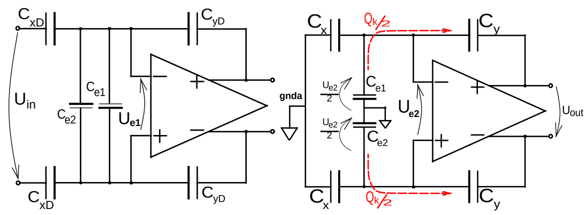
$$U_k = 2.\frac{C_e}{C_y} \cdot \left(U_{e1} - \tfrac{1}{2}U_{e2}\right) \qquad (7)$$

To completely compensate for all arising errors this voltage U_k has to be equal to the error term in eq. (1):

$$2.\frac{C_e}{C_y} \cdot \left(U_{e1} - \tfrac{1}{2}U_{e2}\right) = U_{e2} \cdot \left(1 + \frac{C_x}{C_y}\right) \qquad (8)$$

and a general formula for the C_e-value can be derived:

$$C_e = \left(C_x + C_y\right) \cdot \frac{U_{e2}}{\left(2.U_{e1} - U_{e2}\right)} \qquad (9)$$



a) error measure phase **b)** compensation phase

Fig.4: Charge addition based SC error compensation.

Assuming the idealisation that $U_{e1} \approx U_{e2} \approx U_e$ results in a sizing $C_e \approx C_y + C_x$ for an integrating SC amplifier in Fig.1. If $U_{e2} > U_{e1}$ (e.g. low amplifier gain G < 60 dB or large charge withdraw into C_e), the error compensation can be fine tuned by choosing C_e-value slightly larger than ($C_y + C_x$) in eq. (9). With $U_{e2} = U_{e1}.(1+\varepsilon)$ from equation (4) follows:

$$C_e = 2 \cdot C_x \cdot \frac{1+\varepsilon}{1-\varepsilon} = 2 \cdot C_x \cdot \left(1 + \varepsilon'\right) \qquad (10)$$

with $\varepsilon' << 1$. In our design procedure for the cyclic ADC the exact assignment for ε' has been made by transistor-level simulation, which allowed us to compensate additionally for other charge leakage originating from some second order effects.

Proceeding with the error calculation we can establish a relative error quotient δ_r dependence on the OpAmp gain G and capacitance ratio $\alpha = C_e/C_x$, for $C_y = C_x$:

$$\delta_r = \frac{\Delta U_{out}}{U_{out}} = \frac{U_{out} - {C_x}/{C_y}\, U_{in}}{U_{out}} =$$

$$\delta_r = \frac{2\alpha^2 - 6\alpha - G\alpha - 4 - 2G}{G(4\alpha + 2 + G)} \qquad (11)$$

Choosing an OpAmp's gain, e.g. 80 dB, and demanding the error to be zero ($\delta_r = 0$), yields the exact value for $\alpha = C_e/C_x = 2.002403$. By designing the error capacitors C_{ex} twofold the value of C_x, C_y instead of 2.00243 the relative error δ_r still remains below $-0.23976.e^{-6}$ which corresponds to – 132.4 dB THD or 21.99 bit of accuracy. Likewise, other conclusion can be drawn concerning mismatch of the C_e-value relatively to C_x, C_y. Even if $C_e = C_x = C_y$ (50% value deviation) the 'miscorrected' SC operation is still twofold (1bit) more accurate than in uncorrected case. A disadvantage of the charge correction compared to voltage correction as in [1],[2] is a charge wastage from the measuring capacitors C_e during every correction phase. However, all C_e can be designed large enough to correct all errors of a multi-phase regime in the final phase.

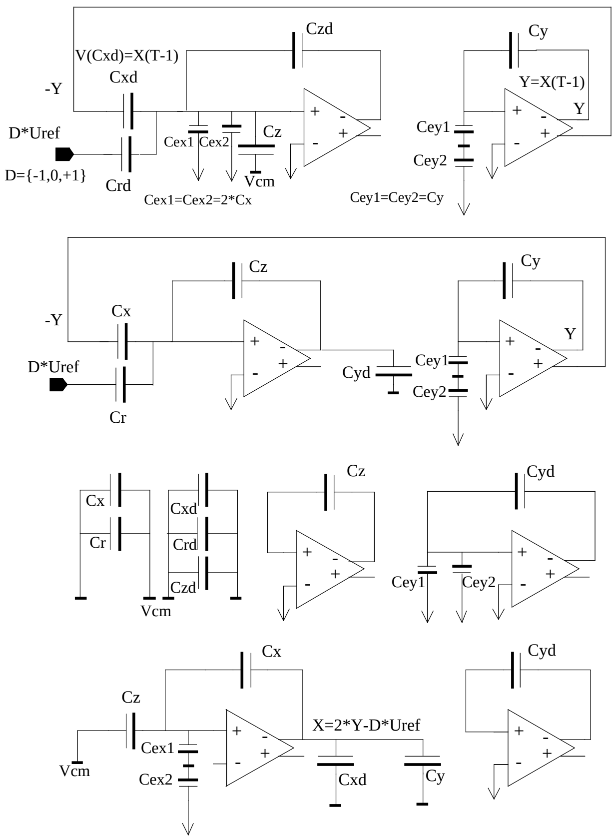


Fig.5: Four-phase SC implementation of an 1-bit conversion cycle in the 2nd ADC prototype.

SC implementation of the cyclic ADC

In our first cyclic ADC design attempt [4], we implemented the conversion algorithm using OpAmps with 100 dB gain and a voltage addition correction similar to Fig.3, however, unlike in [1] and [2] the SC phase count per 1-bit conversion cycle has been reduced to three, by merging the error measuring and the sampling phases together, to increase the ADC's sampling rate. Consequently, an approach circumventing the prediction phase constrained us to choose the error measuring capacitors as $C_e = 0.1C_x$ not to burden much the sampling process in the working capacitors C_x, C_y by a leakage wastage into C_e. The chip test results showed a considerable sampling noise on C_e disturbing completely the results. In avoidance of additional sampling noise in the voltage addition correction therefore the value of error sensing C_e should not be considerably smaller than C_x, C_y. Nevertheless, by deactivating the analog correction the ADC achieved 10 bit linearity and spectral purity.

The second design with 85dB-OpAmps uses a correlated double sampling (CDS) [5] and the novel charge-based error compensation. There are four SC phases per 1-bit cycle, this number being determined by the SC block performing the mathematical function ($2 \cdot X_i \pm U_{ref}$) (Fig.5, left-hand-side-block). Two of these phases (2 and 4) are charge transfer integration processes, which must be corrected.

The predictive, first phase is identical to phase 2 except of the error-sensing capacitors at OpAmp's input. The error stored at these C_{ex} (4 pF) during the prediction phase is not used for correction until the final phase 4. In phase 2, the signal multiplication with a factor of 2 is achieved by charge redistribution from C_x to C_z relatively to $-X_i$, the negative residue signal from preceding bit-cycle (cross-coupled fully differential outputs [1]). The correction in phase 2 relies on a capacitance C_z being re-used as integration capacitance, after serving as a measuring capacitance during phase 1 where it was charged up to the negative equivalent of the error U_{e1}. Since in this phase the output voltage is used only for an imprecise charging of the S&H dummy capacitor, we do not need to compensate for both error terms in equation (1), but only for the charge transfer error share (first term). Therefore only half the charge amount from equation (2) is required, and consequently the value of C_z can identical to C_x (2 pF), which among others is required also for the integrator gain = 1. The third phase accomplishes just a simple reset suspending any error compensation. Finally, in phase 4 the capacitor mismatch between C_x, C_z is cancelled by charge re-transfer and the accurate output voltage is provided for the subsequent calculation (S&H block). This means that the whole equation (1) applies, and therefore the errors are compensated by charge addition from twofold-sized $C_{ex1,2}$ according to equation (2). The mismatch between the reference C_r and the sampling C_x capacitors is cancelled in a dummy half-cycle at the beginning of A/D conversion by sampling the ADC input U_{in} onto C_r and transferring it to C_x. Likewise, this dummy cycle is performed with offset and finite gain error correction.

The second SC block shown right hand side in Fig. 5, forming a 3-phases sample-and-hold (S&H) circuit, is corrected by means of charge addition from C_{ey1},C_{ey2}.

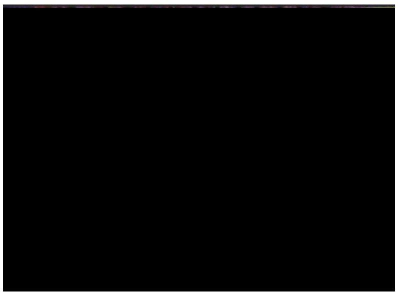


Fig.6: Chip photograph of the 2nd ADC prototype in 0.6µm CMOS X-FAB process in 1.3 mm² chip die.

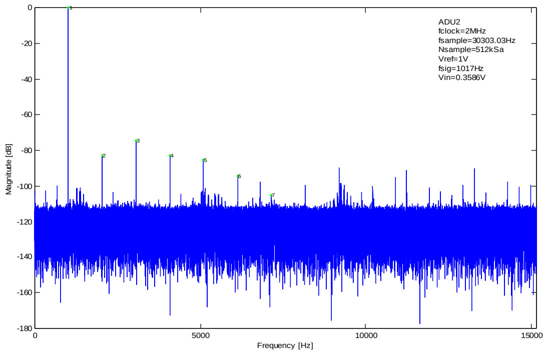


Fig.8: Spectral plot of the 2nd ADC for 1kHz sinus and 2MHz clock (30.3kS/s) and full-scale input (1V) featuring 66.34 dBc SINAD and –74.36 dBc THD.

Analysis and achieved results

The correction principle employed in the second ADC prototype proved functional as soon as the first dynamic and static measurements were taken. The characterisation of the ADC took place down to 16bit-level resolution. The charge based analog correction improves the suppression of harmonic distortion, so that the original THD of –69.8 dB changes to –74.4 dB, thus positively affects the overall ADC performance by increasing the SINAD (Noise & Distortion) from 65.77 dB to 66.8 dB, as shown in Fig. 8 at corresponding test set-up. This corresponds to an effective resolution of 10.8 bit. Furthermore, as the noise floor (SNR = 67.6 dB) represents the lower bound for increasing this ADC's accuracy it is to be expected that a noise optimisation centred redesign would further improve the ADC. The integral non-linearity (INL) is found to meet the requirements for a 12-bit level accuracy within ± 0.5 LSB, as shown in Fig. 9. Static measurements not only show a lessening of non-linear distortion but also a reduction of the ADC's offset from initial 300 – 600 LSB units down to only 20 LSB units when using analog correction.

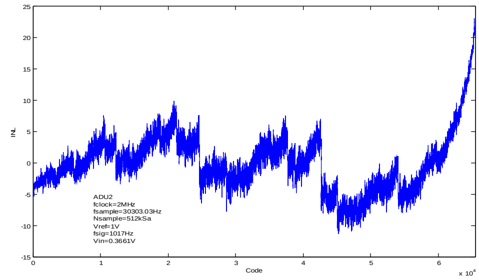


Fig.9: INL plot at identical test set-up to Fig. 8.

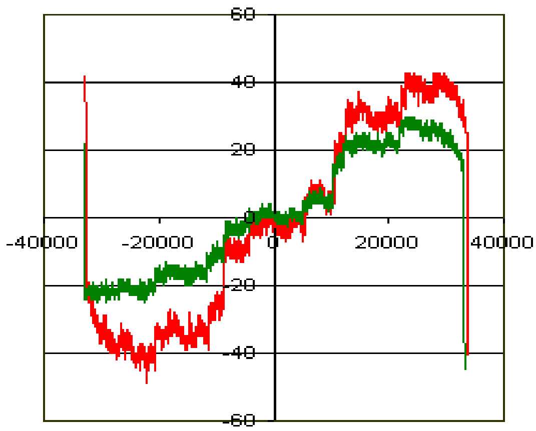


Fig.10: Comparison of LSB-error plots (beside a curve slope, the nonlinearity and the offset included,) while analog correction On (green) and Off (red).

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*) variable U is here used for voltage for consistency with figures which were generated in German.

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