Evaluation of time resolution of NMOS sampling switches

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Summary

Usually in CMOS line receivers and downconversion mixers, a key component is the NMOS sampling switch. When designing sampling switches, one has usually to trade off resolution against bandwidth and aperture time. In this perspective, we modeled the aperture time of the NMOS sampling switch for low swing voltage signals taking also into account the dependence of the threshold voltage on the body effect. Then we compared the aperture time behaviour using three submicron CMOS technologies (0.8, 0.5 and 0.25 µm minimum channel length respectively). The results indicate that an aperture time of about 100 ps is achievable with a CMOS 0.25 µm minimum channel length technology working at low supply voltage.

Keywords

Aperture time, CMOS integrated circuits, high-speed integrated circuits, sample and hold circuits, A/D converters.

Introduction

Let us consider the basic NMOS sampling switch of Fig. 1 (i.e. Sample and Hold circuit).

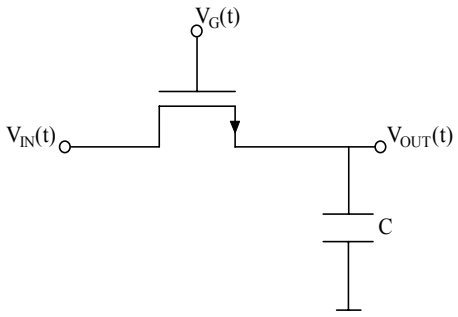

Figure 1: NMOS sampling switch.

The circuit fetches the input signal $V_{IN}(t)$ and stores it during full A to D conversion. As long as the switch is closed, the voltage across the hold capacitor C follows the input voltage $V_{IN}(t)$. When the switch opens, the voltage across C (i.e. $V_{OUT}(t)$) is frozen: while the switch is opening, the connection between C and the input weakens so that the final voltage across C is an average of the input signal throughout the opening time (i.e. the aperture time, t_a in the following of the paper). The model of the aperture time that we will introduce in the next section, is based on this intuitive view. The relation between resolution N (where N defines the resolution, i.e. number of bits, of the converter), f (where f is the frequency of an ideal input sine wave) and t_a of a sampling switch is given by [1]:

$$t_a = \frac{2^{-(N+2)}}{\pi f} \qquad (1)$$

One of the most stringent requirements for sampling circuits is related to the aperture time of the sampler; then from the above equation, given the value of t_a we can estimate the resolution N at a given input sine frequency f and vice versa. An illustration of the above equation is given in Fig. 2: for instance, for sampling a 1 Vpp, 1 GHz sinusoid with 12-bit resolution, the aperture time should be < 250 ps [2]. Using an NMOS transistor, with a minimum channel length of 0.8 µm, GHz sampling frequencies can be achievable [3].

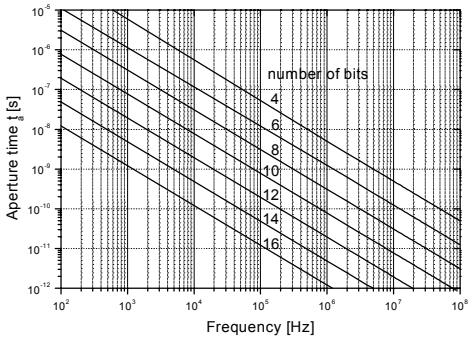

Figure 2: Relation between resolution, bandwidth and aperture time (eq.(1)) [1].

In this paper we model the aperture time and evaluate the time resolution of NMOS sampling switches at high operating speed for three different CMOS submicron technologies (i.e. with minimum channel length of 0.8μm, 0.5 μm, 0.25 μm respectively). On the basis of the approach presented in [3], we take also into account the dependence of the threshold voltage on the body effect. We evaluate the time resolution with respect to the swing of the input signal, the supply voltage value and the width of the sampling transistor.

The paper is organized as follows. In the next section the derivation of the aperture time model for the NMOS sampling switch is presented. We implemented the model in MATLAB and then the results of our analysis are reported and discussed. Finally the conclusions are drawn.

Model formulation

Let us consider the basic NMOS sampling switch of Fig. 1 and some properties of the sample-and-hold circuit as shown in Fig. 3.

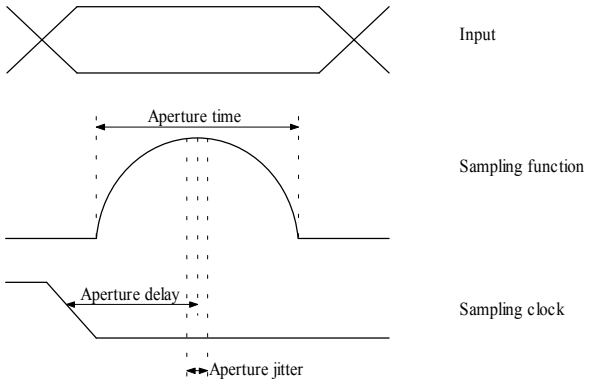

Figure 3: Definition of some properties of a sample-and-hold circuit.

A sample can be considered as the weighted average input signal: the weight function is the so-called sampling function (SF). The sampling happens when the sampling function reaches its maximum value. The time duration of the most significant part of the sampling function is the aperture time (or aperture window width). The aperture delay is the time elapsed from the sampling edge of the clock to the actual moment when the sample is taken, i.e., the middle of the aperture window. We take into account no aperture jitter or aperture uncertainty (i.e. uncertainty of the sampling moment). Following [3], we introduce the basic concept of the sampling function and, starting from this, of the aperture time, t_a. We are concerned with low swing signals, then we assume that the drain-source voltage is small and that there is no clock feedthrough: these assumptions can cause reasonable errors. The gate voltage is a function of time (linear slope):

$$V_G(t) = \begin{cases} V_{DD} & se \quad t < t_0 \\ -V_{DD}\,\dfrac{t}{t_0} & se \quad -t_0 \le t \le 0 \\ 0 & se \quad t > 0 \end{cases}$$

Input and output voltages are expressed as: $v_{IN} = V_{DC} + v_{in}$, $v_{OUT} = V_{DC} + v_{out}$, where v_{in} , v_{out} are the small signal voltages and V_{DC} is the dc-bias of the input and output voltages. Due to our assumptions (small value of V_{DS}) the transistor is assumed to operate in non-saturation until it is turned off. The large signal drain current is:

$$i_D = \begin{cases} \beta\left[(v_{GS} - V_T)v_{DS} - \dfrac{1}{2}(v_{DS})^2\right] & if \quad v_{GS} \ge V_T \\ 0 & if \quad v_{GS} < V_T \end{cases}$$

where $\beta = \mu C_{OX}\dfrac{W}{L}$ and the meaning of the parameters in the previous equations is the usual one. The threshold voltage is given by:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right)$$

where V_{T0} is the zero bias threshold voltage, γ is the body factor, $2|\phi_F|$ is the surface inversion potential and v_{SB} is the large signal source-bulk voltage.

In [3], the expression of v_{out} is computed considering the threshold voltage as constant. In our analysis we disregard this assumption and consider the threshold voltage as a function of the input signal value through the body effect. We need the expression of v_{OUT} after the sampling time to compute the sampling function. After sampling the output voltage is constant (the transistor is turned off) and v_{sample} is the integral over all the previous values of the input multiplied by a weight function (i.e. the sampling function):

$$v_{sample} = v_{OUT}\left(-t_0\,\frac{V_{DD} + V_T}{V_{DD}}\right) = \int_{-\infty}^{+\infty} v_{IN}(\tau)h(\tau)\,d\tau$$

where $h(\tau)$ is the sampling function. Both the expressions of v_{OUT} and $h(\tau)$ are rather complex: we don't report them for the sake of simplicity. If charge injection effects are neglected, the input and output voltages after sampling are equal, then if the input value is, let say k, we can write

$$k = \int_{-\infty}^{+\infty} kh(\tau)\,d\tau \text{ and then } 1 = \int_{-\infty}^{+\infty} h(\tau)\,d\tau$$

If $v_{IN}(t) = V_{SWING} \times u(t)$, where u(t) is the unit step function, it can be demonstrated that:

$$h(\tau) = -\frac{i_D(\tau)}{V_{SWING}\, C}$$

This is a very powerful result: in fact, to compute the sampling function, we only need to know the expression of the current in the sampling switch when the input signal is the step function. The aperture time is defined as the width of the peak of the sampling function where 80% of the sensitivity is confined: $t_a = t_{90} - t_{10}$ where the times t_{10} and t_{90} are defined as:

$$0.1 = \int_{-\infty}^{t_{10}} h(\tau)\, d\tau \qquad 0.9 = \int_{-\infty}^{t_{90}} h(\tau)\, d\tau$$

We allow a maximum attenuation of the signal of 20% through the sampling switch due to aperture effects. The sampling time value results to be strongly dependent on the value of t_0. In our analysis, we take into account also the dependence of V_T on v_{SB} through V_{SWING}. This effect was not taken into account in [3].

Simulation results

We implemented the model presented in the previous section in MATLAB.

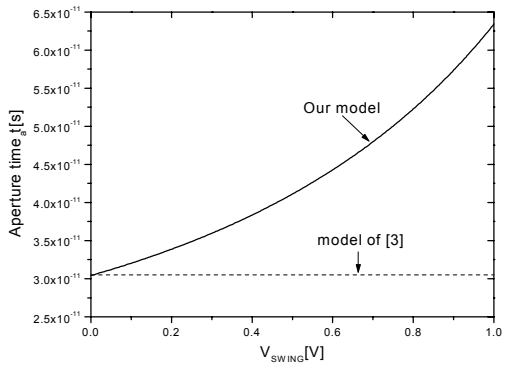

Figure 4: Aperture time t_a of the sampling circuit against V_{SWING} with 0.24µm technology. The values of the parameters are: C = 20fF, W = 5µm, t_0 = 100ps, V_{DC} = 0.5V, V_{DD} = 1.4V e L = 0.25µm**.**

In Fig. 4, the aperture time t_a as function of the value of V_{SWING} is shown. As it can be seen, the aperture time value is strongly dependent on the value of V_{SWING}; while in [3] the aperture time was constant with respect to V_{SWING}. More precisely, for a fixed value of V_{SWING}, the aperture time assumes a value greater than the value given by the model of [3]. Then, for a fixed value of the input sine wave frequency, the converter resolution decreases (see Fig. 2).

In Fig. 5, the aperture time t_a against the power supply value, taking into account three submicron technologies, is shown. The values of the gate lengths are the minimum allowed for the given technologies. All other parameters are constant. The value of W has been set to 2 µm that is the minimum channel width for the CMOS AMS CYE 0.8 µm technology.

The aperture time is strongly dependent on the power supply value when considering the AMS technology while it is less dependent when considering the ATMEL technologies. Best performances are obtained by the ATMEL 0.24 µm technology: t_a is in the order of 100 ps even at low supply voltage (e.g. 1.4 V). If zero aperture-jitter is assumed, this indicates the possibility of single bits sampling at 10 Gs/s (with $f \approx 4\ 10^8$ s) even at 1.4 V power supply.

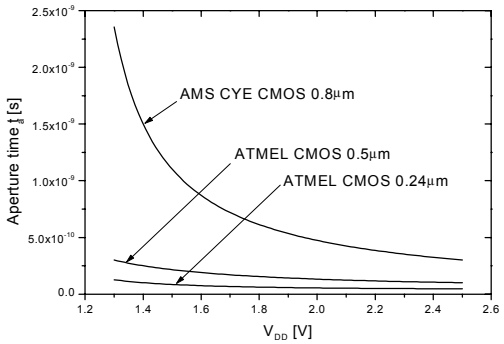

Figure 5: Aperture time t_a as function of the power supply value. The values of the other parameters are: C = 50 fF, W = 2 µm, t_0 = 100 ps, V_{DC} = 0.5 V, V_{SWING} = 0.5 V.

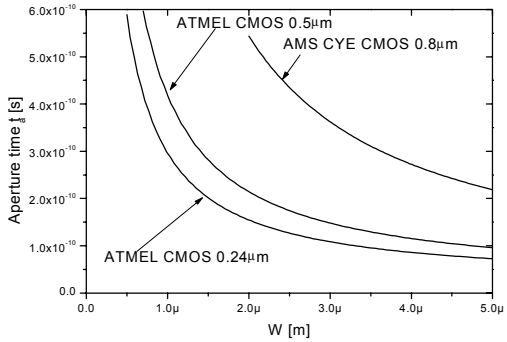

Figure 6: Aperture time t_a as function of the sampling transistor width. The values of the other parameters are: C = 50 fF, t_0 = 100 ps, V_{DC} = 0.5 V, V_{SWING} = 0.5 V, V_{DD} = 2.5 V.

In Fig. 6, the aperture time t_a against the width of the sampling transistor is reported. Please take into account that the minimum transistor widths are the following: AMS CYE 0.8µm W_{MIN} = 2µm, ATMEL 0.5µm W_{MIN} = 0.7µm, ATMEL 0.24µm W_{MIN} = 0.5µm. All other parameters are constant.

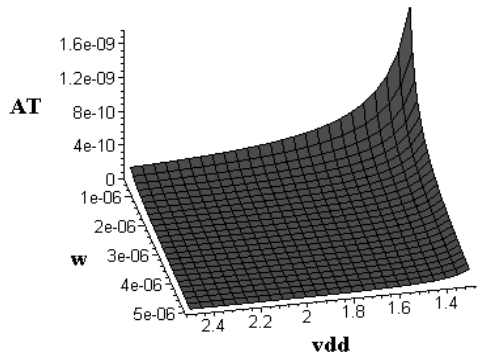

Figure 7: Aperture time (AT) as function of the sampling transistor width and the power supply value with 0.24µm technology. The values of the other parameters are: C = 50 fF, t_0 = 100 ps, V_{DC} = 0.5 V, V_{SWING} = 0.5 V.

Fig. 7 shows that the aperture time increases at low supply voltages and with small sampling transistor widths, using ATMEL 0.24 µm technology. Moreover it can be seen that, for instance, a sampling frequency of 10 GHz (t_a = 100 ps) can be achieved with a power supply of 1.4V and a sampling transistor width of 4µm.

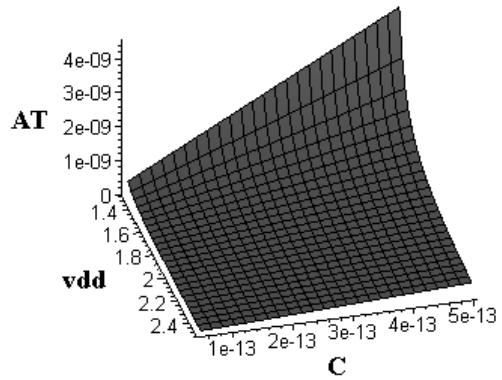

Figure 8: Aperture time (AT) as function of the hold capacitor and the power supply value with 0.24µm technology. The values of the other parameters are: L = 0.25µm, t_0 = 100 ps, V_{DC} = 0.5 V, V_{SWING} = 0.5 V, W = 2µm.

Please take into account that, as it can be seen from Figs. 5 and 6, for all the given technologies, t_a increases at low supply voltage and with small sampling transistor widths.
In Fig. 8, the aperture time against the power supply Vdd and the hold capacitor C values is plotted.

Conclusions

It has been shown [3] that, when NMOS sampling switches are operated with low swing signals, the switch can be modeled as a device which determines a weighted average over time of the input voltage signal. Starting from this result, we implemented in MATLAB a model of the NMOS sampling switch more general than the one presented in [3]: the results indicate that the aperture time is dependent to V_{SWING} and this behavior affects the converter resolution negatively. We made also some comparisons considering three CMOS submicron technologies, evaluating the aperture time against the power supply voltage and the sampling transistor width. The results indicate that, using a 0.24 µm minimum channel length technology, sampling speed of 10 Gb/s can be achieved at low supply voltage (i.e. 1.4 V).

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References

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