Novel pipelined switched-current A/D converter for smart sensors

I. Vecera [1)], R. Vrba [2)]

[1)] SCG CDC, B. Nemcove 1720, 756 61 Roznov pod Radhostem, Czech Republic, phone +420 651 667178, e-mail: ivo.vecera@onsemi.com

[2)] Brno University of Technology, Department of Microelectronics, Údolní 53, 602 00 Brno, Czech Republic, phone + 420 5 41146161, e-mail: vrbar@umel.fee.vutbr.cz

Summary

This paper describes pipelined switched-current A/D converter designed in 0.6μm BiCMOS technology. Modified conventional-restoring algorithm, called redundant-sign-digit (RSD), was implemented what decreases the amount of high-precision components. Two modes of operation are possible. By changing from pipeline conversion to cycling mode, less power dissipation is obtained at the expense of conversion time. Proposed A/D converter is suitable for conversion of the current with very low amplitude from analog into digital domain. Current mode enables operation down to 3V thus is suitable for battery powered applications. The system integrates band-gap reference and independent supervisory circuit with 1% accuracy. Current consumption in sleep mode is less than 1μA. A/D converter is prepared to meet 1452.2 specifications.

Keywords: SI A/D converter, pipeline architecture, sensor applications

Introduction

A lot of work is being done in the field of analog-to-digital conversion [1],[2]. The steering factor is definitely a rapid accession of low-cost microcontrollers and DSP's in analog world.

Low input impedance is the advantage of current mode compared to voltage mode due to increased noise immunity. It makes such approach suitable for processing of sensor signals.

Current processing is based on current mirrors [3],[4]. In MOS technology where their use is significant, the design must be very careful according to mismatch thus their required large dimensions can become limiting factors when speaking of the die size.

Switched-current techniques overcome this side effect since the mirroring is done on one MOS transistor and the only resolution of the gate-charge sampling is important.

On the contrary to most voltage-mode types of

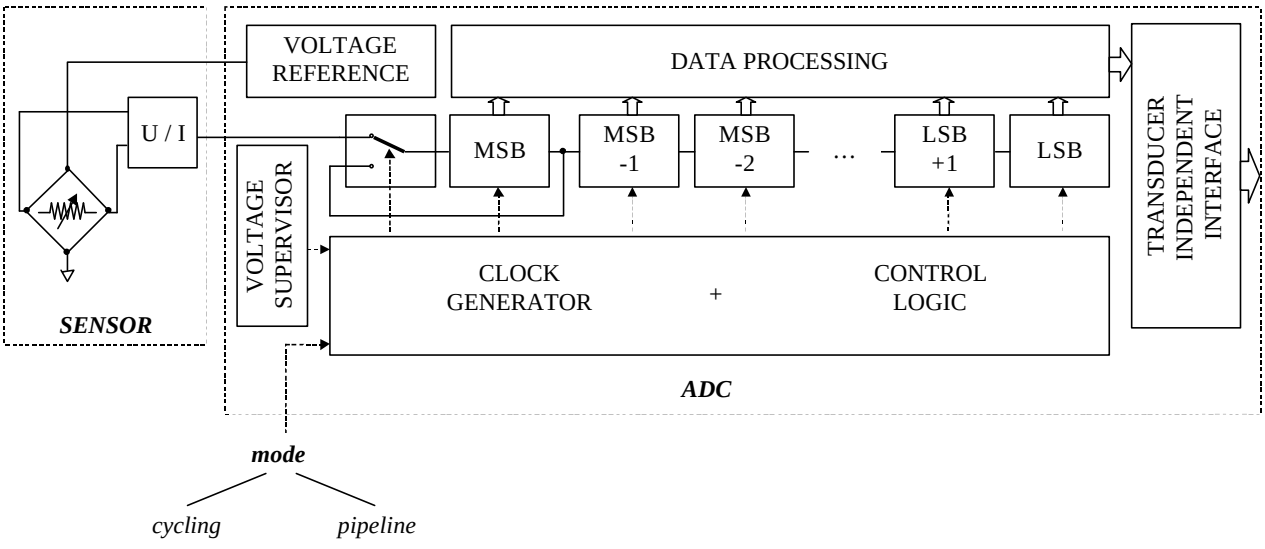


Figure 1 Block diagram of the proposed algorithmic A/D converter

converters [1], switched-current technique does not require either high precision resistors or capacitors thus it is compatible with standard CMOS processes.

System description

Algorithmic A/D converter, as illustrated in Figure 1, consists of *N* algorithmic cells for bit generation. The digital data are present in RSD code form. Conversion starts from MSB to LSB. Pipelined data are latched and used for further data processing to reproduce binary form of the digital code. Finally, these digital data are formed in the TII (transducer independent interface) block for coupling with the outside world.

Independent supervisory circuit which is implemented in the architecture, scans supply line voltage for minimum required 3V, ensures correct start-up and via its input interface also changes the mode of operation among shutdown, idle (cycling conversion) and active (pipelining). It is directly linked with the control logic and clock-generator circuit to synchronize the conversion process Internal 1.25V band-gap reference can be used by the user for providing temperature-independent signal.

ADC architecture

The A/D conversion of the proposed ADC (Figure 1) is based on an RSD algorithmic conversion. The conversion is based on the multiply-by-two method and is similar to conventional restoring (CR) algorithm described by the following Equation 1:

$$Y = q\sum_{i=0}^{N-1} a_i 2^i = \frac{Y_{FS}}{2^N} 2^{N-1}\left(a_{N-1} + \frac{1}{2}\left(a_{N-2} + \ldots + \frac{1}{2}(a_0)\right)\right)$$

where q is quantizing step, Y_{FS} is full-scale input

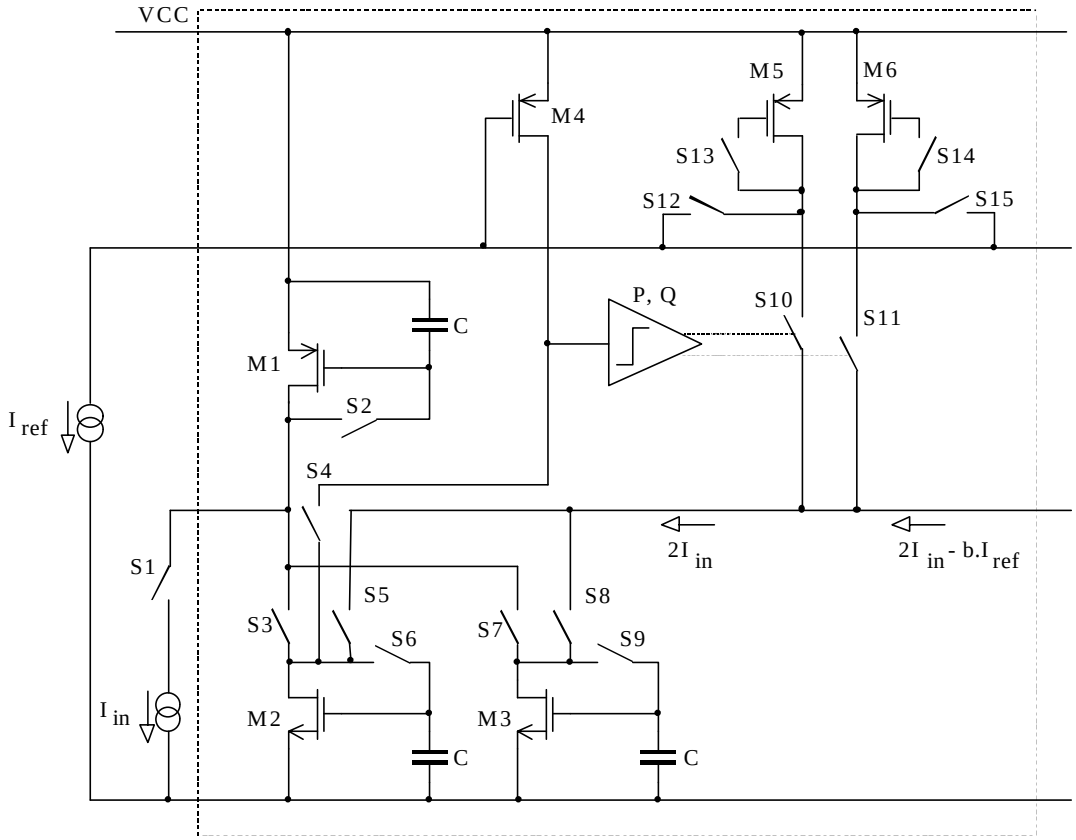
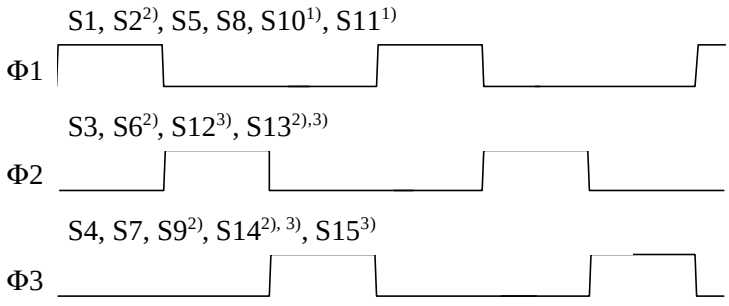


Figure 2: Schematic of one cell of the SI A/D convereter



[1)] switches controlled by comparator outputs P and Q
[2)] fine timing adjustment needed to eliminate gate-capacitor charge error
[3)] special control in pipeline mode – switches activated each n[th] period

Figure 3: 3-phase timing of switches in the algorithmic cell

signal and a_i is the digital code from the i^{th} cell, having value 0 or 1.

In RSD algorithm, the Eq. 1 is modified, employing the digital code b_i which can take value 0, 1 or 2.

The ADC can operate either in pipeline or cycling mode. Pipeline *N*-bit conversion employs *N* algorithmic cells. Cycling conversion is reduced to MSB cell while the resting *N-1* cells are in power-save mode and the analog output signal from MSB cell is folded back to its input to generate less significant bit. The conversion time is then *N* times longer than the pipeline conversion time since the conversion in MSB cell continues until least-significant bit is produced. This mode is beneficial when low power consumption is required (for example in idle signal monitoring) to help increase battery run times.

RSD algorithm and its realization

RSD algorithm as well as CR algorithm is based on multiply-by-two method and reference signal subtraction. Operation provided in i[th] algorithmic cell can be described by the Eq.2 (for CR) and Eq.3 (for RSD):

$$I_{out\_CR} = 2I_{in} - a_i I_{ref\_CR} \quad (2)$$

$$I_{out\_RSD} = 2I_{in} - b_i I_{ref\_RSD} \quad (3)$$

The relation between reference currents is

$$I_{ref\_CR} = 2I_{ref\_RSD} \quad (4)$$

and since I_{ref_CR} corresponds full-scale value, I_{ref_RSD} is equal to half of the full scale. By employing two reference currents, non-critical comparison can be performed when the processed signal is close to half of the full-scale, thanks to finer subtraction; by ensuring the same converter resolution. The circuit realization is shown in Figure 2. The input signal, I_{in} can take on any value between zero and $2I_{ref}$. During the conversion, the converter's switches are controlled by clock signals shown in Figure 3.

The cell conversion period takes 3 phases, Φ1, Φ2 and Φ3. It is initiated in phase Φ1 by closing switches S1 and S2, causing the current I_{in} to be stored in M1 by settling the gate voltage on M1. During the next phase (Φ2), S3 and S6 switches are closed (S1 and S2 opened) to reproduce stored current from M1 to M2. Then by opening S3 and S6 and by closing S7 and S9, phase 3 continues to set the same current on M3.

In parallel to that (phase 3), stored current on M2 is compared with two non-critical values P and Q (close to I_{ref}), derived from reference current I_{ref}. The comparator output is latched and during the last phase (Φ1) enables or disables switches S10 and S11, according to whether the decision level P and Q was lower than I(M2) or higher, respectively.

In this way, subtraction $2I_{in}$ - $b.I_{ref}$ is performed (switches S5 and S8 are closed) during Φ1 and the resulting signal acts as the input for the next cell (while the new value of the input current I_{in} is loaded into M1) in the pipeline mode or is fed back into M1 of the same cell in the cycling mode.

Reference current

Reference-current reproducibility (together with switched-current-mode side effects that are widely discussed in [3], [5]) plays a key role in the resolution of the converter. The reference current is stored also in the memory cells (M5 and M6 in Figure 2) and its charge refreshment is provided periodically and sequentially for each algorithmic cell during the phase Φ1 and Φ2, respectively, when the current sources are inactive.

Conclusion

Proposed RSD algorithmic A/D converter was designed in 0.6μm BiCMOS technology and the example of the simulated results is shown in Figure 4. Bottom left picture shows copying of the current in the P-memory cell (M1) during phase Φ1 and in the middle and top there is sampling of the gate-charge on the transistors M2 and M3, respectively. Right panel displays corresponding propagation of the current: The input current is stored in M1 memory cell during time frame I, it is copied onto M2 and M3 transistors during II and III and them doubled signal is sent back into M1 again with no subtraction during IV.

Simulation results show that for input currents in the range between 0 and 10μA and bias current of 1μA, 9-bit resolution can be achieved at sampling rate up to 200kHz.

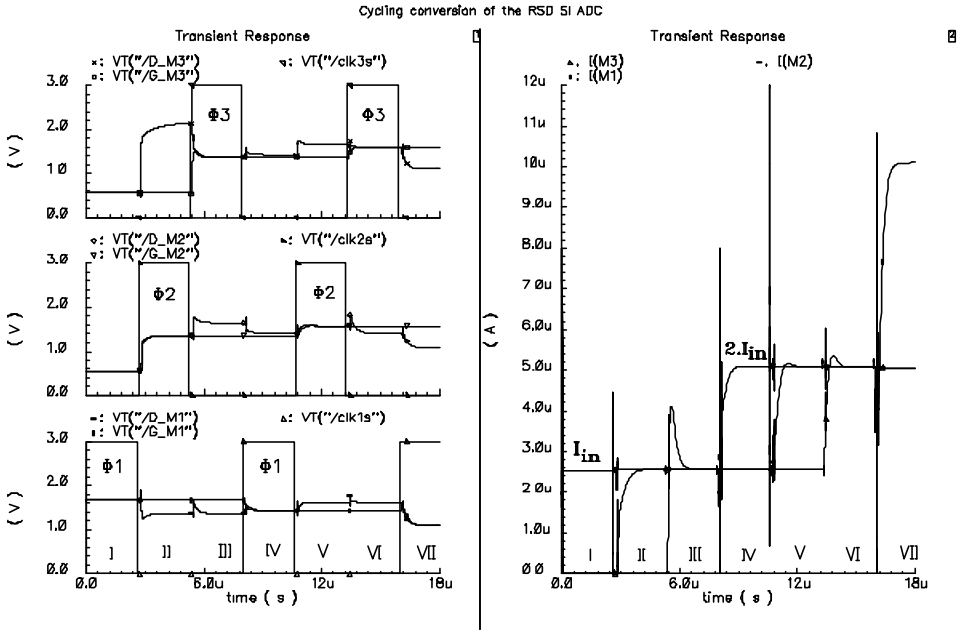


Figure 4: Simulated settling of the gate potential (on the left) during three phases of the RSD algorithmic conversion and corresponding multiplication of the current (on the right)

References

[1] R.K. Hester, M. de Wit, S. Kiriaki, 'Fully Differential ADC with Rail-toRail Common-Mode-Range and Nonlinear Capacitor Compensation', IEEE JSSC, vol. 15, pp. 173-183, February 1990

[2] P. Real, H. Robertson, Ch.W. Mangelsdorf, T. L. Tewksbury, 'A Wide-Band 10-b, 20-Ms/s Pipelined ADC Using Current-Mode Signals', IEEE JSSC, vol. 26, pp. 1103-1108, August 1991

[3] R.S. Soin, F. MAloberti, J. Franca, 'Analogue-digital ASICs - circuit techniques, design tools and applications', Peter Peregrinus Ltd., London, 1991

[4] C. Toumazou, F.J. Lidgey, D.J. Haigh, 'Analogue IC design: the current-mode approach', Peter Peregrinus Ltd., London, 1990

[5] T.S. Fiez, G. Liang, D.J. Allstot, 'Switched-Current Circuit Design Issues', IEEE JSSC, vol. 26, pp. 192-201, March 1991