Combining DACs for Improved Performance

K. Ola Andersson[1,2], Niklas U. Andersson[1,2], Mark Vesterbacka[1], and J. Jacob Wikner[3]
[1]Dept. of E.E., Linköping University, 581 83 Linköping, Sweden, fax +4613139282
[2]LiDC, Ericsson Microelectronics AB, Box 1554, 581 15 Linköping, Sweden
[3]SDC, Ericsson Microelectronics, Westmead Dr., Swindon, SN5 7UN, UK, fax +441793490151
E-mail: {olaa, niklasa, markv}@isy.liu.se, jacob.j.wikner@mic.ericsson.se

Summary

This work is an overview of recently proposed methods on combining DACs in order to improve performance. Some further development of these techniques are also presented. The techniques aim at reducing glitches and sensitivity towards limited output impedance in current sources.

Keywords: D/A conversion, glitches, nonlinearities

1. Introduction

Today's telecommunication applications require high-speed and high-resolution data converters. In, e.g., digital subscriber line (DSL) applications the requirements on the digital-to-analog converter (DAC) is in the order of 12-14 bits of resolution and several MHz of signal bandwidth. These requirements are not always easily fulfilled, and in this work we give an overview of some recently proposed techniques utilizing several sub DACs combined into one DAC for improved performance.

The current-steering approach (see Fig. 1(a)) is often used in high-speed applications, since the architecture enables fast operation. The performance is however often limited by linearity problems. Mismatch between the transistors in the current sources causes errors in the bit weights and limits the static linearity of the DAC. To solve this problem calibration or randomization techniques, so called dynamic element matching (DEM, see e.g. [1]), are often suggested. In some applications distortion is more crucial than the noise, especially in oversampled systems where much of the noise typically can be filtered out. DEM techniques utilize redundant codes and randomization to transform distortion into noise with the benefit of linearizing the device but introducing more switching activity and hence noise. There are schemes to minimize the glitching activity and still maintain a reasonable amount of randomization [2, 3]. It is also known that the glitching activity is reduced by using special codes, such as segmentation of the MSBs or other arrangements. In this work we overview different ways to combine a pair of converters to reduce the glitches to a relatively low (digital) hardware cost. In Sec. 3 we highlight an example where the converters are linearly coded [4] yielding low glitch errors.

For higher signal and updating frequencies dynamic errors tend to be the limiting factor on the linearity. One source of dynamic nonlinearity is the nonzero output capacitance of the current sources, causing signal dependent settling errors, which in turn yields an overall nonlinear behavior. This phenomenon was modeled with Matlab in [5]. The equivalent circuit representation of that Matlab model is shown in Fig. 1(b). It includes the output capacitance and resistance of the current sources, switch resistance, wire resistance and capacitance. In Sec. 4 we give an example on how to use two sub DACs to reduce the distortion due to limited output impedance by introducing redundancy which allows the common-mode signal to be varied.

2. General multi-DAC concept

Assume that we have an N-bit DAC consisting of a set of M parallel sub DACs, with their outputs summed to produce the total output. The number of weights in the sub DACs are chosen so that the overall N-bit resolution can

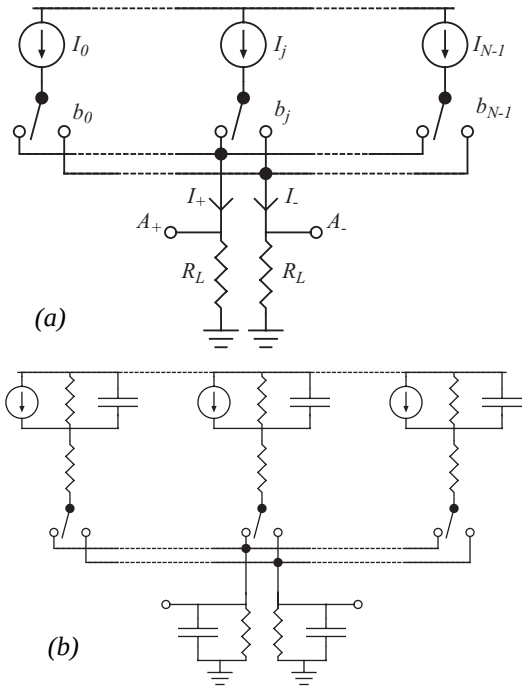

Figure 1: (a) Ideal and (b) model of current-steering DAC including parasitic resistances and capacitances.

be met. The input to each sub DAC is denoted X_m. We let the outputs of the sub converters, A_m^+ and A_m^-, be differential, where $A_m^- = A_m^{\max} - A_m^+$. $A_m^{\max}$ is the maximum amplitude that can be represented by the given sub DAC. The sum of inputs equals the overall input and the sum of the outputs equals the wanted output.

In e.g. [1] investigations are presented on how the influence of analog errors can be spectrally shaped and attenuated in the signal band. The investigations use the concept of DAC banks and then digital encoding circuits to redistribute the signal to the different DACs. As mentioned, the drawback with these methods is the increased switching activity and in e.g. [2] and [3] we find methods to reduce the glitching and still maintain randomization at a reasonable low hardware cost.

3. Combined DACs with small relative glitch error and DEM

In this section we present a DAC architecture that can be used to improve the glitch performance of high-speed and high resolution D/A converters. The basic architecture was previously presented in [4]. In this work we also show how a simple form of DEM can be incorporated in the structure.

3.1 Linear-coded DAC architecture

A linear-coded DAC is obtained by weighting the currents in Fig. 1(a) according to $I_j = (j+1)I_0$, $j = 0, 1, \ldots, n-1$ [4]. An interesting property of the linear-coded DAC is that the glitch magnitudes are small for transitions involving low values, and become increasingly larger for transitions involving higher values. The distribution of glitches is rather different from, e.g., a segmented converter, which has a constant envelope of glitch magnitudes for all values. The property of nonuniform glitch distribution can be utilized to design a DAC with low glitch magnitudes around the DC level, i.e. a DAC with a small relative error with respect to glitches. This is obtained by connecting two linear-coded DACs in parallel according to Fig. 2, where one DAC converts negative values, and the other positive values. Note that the 4:1 multiplexers are used to illustrate the principle. In an implementation they can be simplified to one layer of AND gates.

To explain the function of the combined DAC architecture we set the control input $P(n)$ to zero. The magnitude of the input will be linear encoded. If we have a positive input, then the sign of the input is used to connect the linear-coded word to DAC 2 via the 4:1 multiplexer. Meanwhile, DAC 1 outputs the highest value that can be represented. Assuming a binary-weighted number representation, this corresponds to inverting all bits of a zero as illustrated in Fig. 2. On the other hand, if the input is

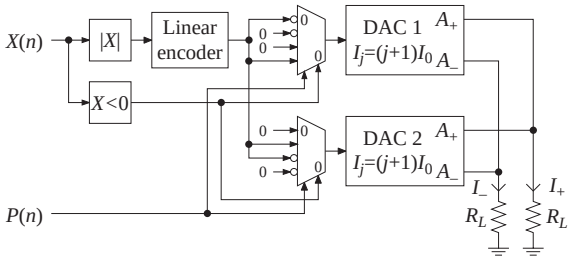

Figure 2: Proposed linear-coded DAC architecture with small relative glitch error and DEM.

negative, the linear-coded word is inverted and connected to DAC 1, i.e. the inversion causes an increase in magnitudes to a corresponding decrease in the output. DAC 2 outputs zero.

The control input $P(n)$ has been designed to change role of DAC 1 and DAC 2 with respect to the sign of the data. Hence, a simple form of DEM can be incorporated in the structure by connecting this input to a pseudo-random binary sequence (PRBS) generator that alternates the use of the DACs randomly. Note that this improvement requires little additional hardware. The overhead is a layer of XOR gates compared with the solution presented in [4], plus the PRBS generator.

3.2 Simulation

To characterize the amount of glitching in the DAC we use a first-order model that considers the glitch magnitude $G(X(n-1), X(n))$ to be proportional to the sum of weights involved in a transition from value $X(n-1)$ to $X(n)$. In Fig. 3 the glitch magnitude is plotted for two 14-bit DACs, where a conventional segmented DAC with seven thermometer-coded most-significant bits is simulated in (a), and the new DAC-architecture is simulated in (b). A ramp with a slope of one has been used as input to both DACs. If larger transitions are investigated, e.g., by increasing the slope, the trend is that the glitch error is increased, but the distribution is similar. The plot indicates that we can expect about the same worst-case glitch magnitudes for both DACs, but a much improved behavior around the DC level for the combined linear-coded DAC architecture.

4. Combined DACs for immunity towards limited output impedance

In this section we present another redundant DAC architecture that can be utilized to limit the impact of finite output impedance in the current sources. This architecture was previously presented in [6], together with a few examples on how utilize the redundancy. In this work we also present a further developed method of utilizing the redundancy.

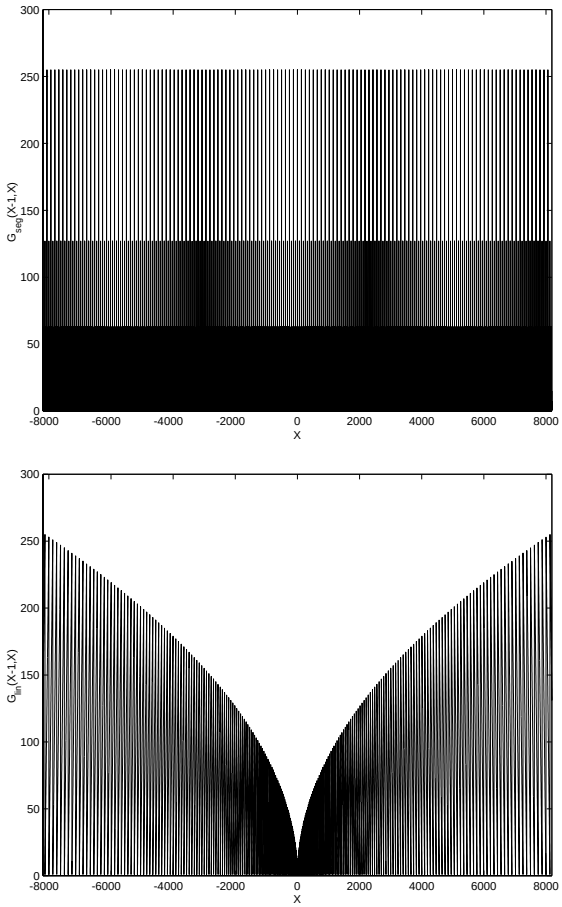

Figure 3: Glitching in 14-bit DACs with (a) conventional 7-bit segmented architecture and (b) the proposed linear-coded architecture.

4.1 Architecture overview

The single-ended output currents for the ideal current-steering DAC in Fig. 1(a) are given by

$$I_+ = I_u \cdot \sum_{i=0}^{N-1} b_i \cdot w_i \text{ and } I_- = I_u \cdot \sum_{i=0}^{N-1} \overline{b}_i \cdot w_i, \quad (1)$$

and the differential output current by

$$I_{diff} = I_+ - I_- = 2 \cdot I_u \cdot \sum_{i=0}^{N-1} b_i \cdot w_i - I_u \cdot \sum_{i=0}^{N-1} w_i \quad (2)$$

where I_u is the unit current, b_i is bit i of the input code X, $\overline{b}_i$ is the inverse of b_i, and w_i is the weight of bit i.

The proposed redundant architecture is shown in Fig. 4, composed of two parallel, nominally identical, current-steering DACs (DAC1 and DAC2). The input signal to DAC*i* is denoted $X_i(n)$, where

$$X_1(n) = X(n) + r(n) \text{ and} \quad (3)$$

$$X_2(n) = X_{max} - X(n) + r(n). \quad (4)$$

$r(n)$ is a control signal and X_{max} is the maximum value of X, which occurs when $b_i = 1$ for all i. If X is binary coded, then $X_{max} - X$ is achieved by inverting all individual bits of X, motivating the inverter symbol in Fig. 4. The A_- terminals of each DAC is connected to a silent DC voltage V_{dump}. With ideal DACs, the control signal $r(n)$ is added to both output currents (multiplied with the gain of the DACs). For the differential current, $I_{diff} = I_1 - I_2$, the same operation as is achieved as before. This architecture is redundant in that there are several ways of representing the differential signal with different common-mode signals, since $r(n)$ is added to the common-mode input signal $(X_1(n) + X_2(n))/2$. One factor that limits the possibly useful control signals is the common-mode rejection of the following circuitry.

In an implementation, the two DACs have to be mutually well-matched, preferably manufactured on the same die, sharing same master bias, etc. It is also important to avoid clock skew between the two DACs, and therefore it is desirable that they share the same clock net. Obvious penalties, compared to conventional DACs are increased area requirements and power consumption

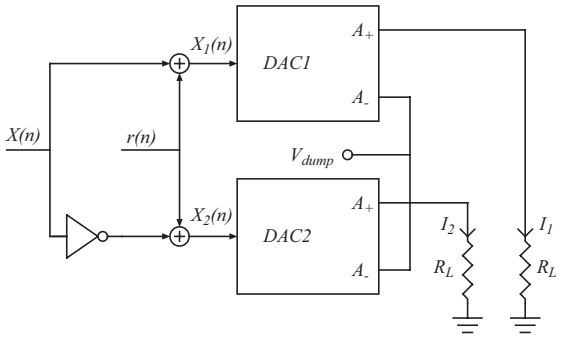

Figure 4: Proposed redundant differential DAC architecture.

4.2 Simulations

One choice of $r(n)$ discussed in [6] is a random dither signal with a given amplitude. This choice of $r(n)$ yields a form of DEM. Another choice that was mentioned in [6], is to choose $r(n)$ as the smallest constant signal avoiding overflow of X_1 and X_2. In this way the parasitic load at the output nodes is lowered. This approach is only applicable to a limited class of signals, i.e., the ones that do not utilize the possible input range, and need to estimate the maximum value of all future samples of the input signal. In this work we modify this approach and instead choose $r(n)$ as the smallest integer fulfilling the boundary conditions

$$r(n) \geq -min(X(n), X_{max} - X(n)) = r_{min}(n) \text{ and} \quad (5)$$

$$|r(n) - r(n-1)| \leq \Delta r_{max} \quad (6)$$

Boundary condition (5) ensures that overflow is avoided, and Δr_{max} is chosen such that the common mode variations can be sufficiently rejected in following circuitry (in the previous approach, $\Delta r_{max} = 0$). The boundary conditions should hold for all n, so we need to keep track of a few future samples of X, otherwise we risk choosing $r(n)$ too small to fulfil both (5) and (6) for some future sample. However, since we need to keep track of less samples than before, this approach is more suitable for an actual implementation.

In Fig. 5(a) and (b) we show simulated 3-tone PSD plots for a single DAC and for the proposed redundant DAC with $r(n)$ chosen as above respectively. The simulation model is a 14-bit binary weighted version of the one presented in [5] (see Fig. 1(b)), parameter values are given in Table 1, and $\Delta r_{max} = 20$. The peak-to-peak value for this particular input signal is approximately 10600, and the spectra have been normalized with respect to the peak power. The largest distortion term is reduced from –72 dB to –82 dB.

Parameter	Value
Output resistance (unit current source)	1 GΩ
Output capacitance (unit current source)	5 fF
Switch resistance (all switches)	100 Ω
Load and wire resistance	100 Ω
Load capacitance	200 pF

Table 1: Simulation parameters and their values.

5. Conclusions

We have presented ideas on how to combine multiple DACs in order to improve the performance in terms of glitches and decreased sensitivity towards limited output impedance.

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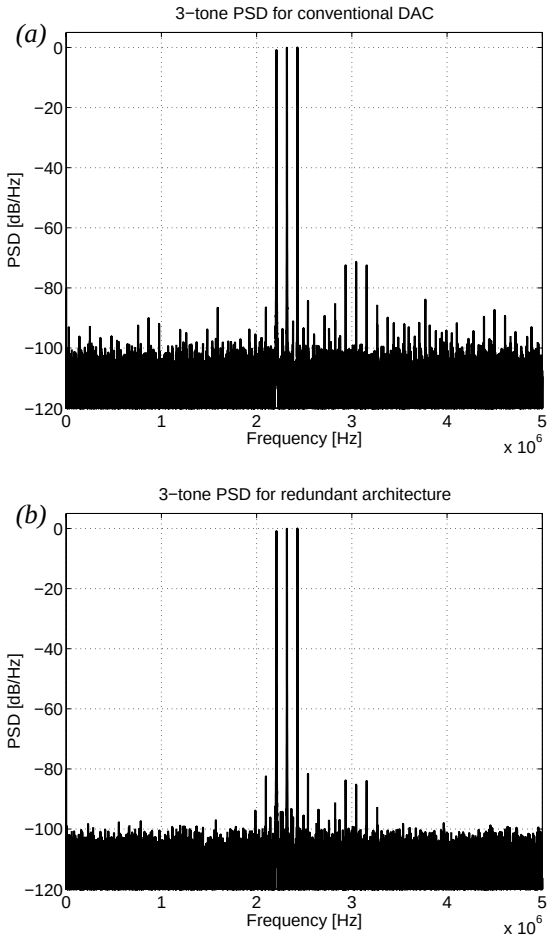

Figure 5: Simulated 3-tone PSD plot for (a) a single (conventional) DAC and (b) the proposed redundant architecture.

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