An Efficient $\Delta\Sigma$ Noise-Shaping Architecture for Wideband Applications

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Summary – In this paper a new optimized multi-stage $\Delta\Sigma$ (Delta-Sigma) structure is proposed. The method combines the reduced-sample-rate architecture with the optimization of the zeros of the noise transfer function (NTF). To achieve this, the first stage of the decimation filter has to be modified as well. Applying this method one can avoid the SNR loss introduced by using the reduced-sample-rate second-stage. The SNR can actually increase for higher-order structures. Simulation results for a 2-0 MASH structure with an oversampling ratio of 4 are shown to verify the technique.

Keywords – multi-stage delta-sigma modulator, MASH, Leslie-Singh, reduced-sample-rate, modified (rotated) sinc filter.

I. INTRODUCTION

Delta-sigma analog-to-digital converters are capable of achieving high resolution in wideband applications. State-of-the-art $\Delta\Sigma$ converters have already been introduced for wideband signals ($f_{\max} \geq 1$ MHz) with more than 12-bits resolution [1], [2]. However, the design of ADCs with high resolution for even higher sampling rate is challenging. To obtain high output sample rate, the oversampling ratio (OSR) must be reduced, and to obtain higher resolution, often multibit quantizer is used in a multi-stage converter ([3, Ch. 7], [4]).

One commonly used architecture is the generalized Leslie-Singh (or an M-0 MASH), which requires a multibit (8-12 bit) quantizer in the second stage clocked by the oversampling clock (Fig. 1). To avoid using very fast and accurate (therefore power-consuming and expensive) ADC's, the reduced-sample-rate architecture shown in Fig. 2 was introduced in [5].

This structure is based on the observation that an Nth-order noise transfer function ($NTF = (1 - z^{-1})^N$) is similar to the denominator of the same order decimation filter, if the filter is the traditional "sinc-type" [6] filter. In this case the denominator of the sinc filter function cancels the digital NTF of the filter following the multi-bit ADC, and one can reduce the clock frequency of the second stage by N (Fig. 2).

However, reducing the sample rate of the second stage by N causes an N-fold increase in the noise power [5], [7], because the order of the decimation filter is the same as that of the modulator. This means that the signal to (inband) noise ratio (SNR) decreases by 3 dB for each doubling of N. In the following, an optimizing technique is introduced which can avoid this SNR loss. In fact, in higher-order cases it can increase it over the SNR of the original (full-speed second-stage) system.

II. OPTIMIZED TRANSFER FUNCTION

In the ideal case, the output of a two-stage modulator contains only the input signal and the quantization noise of the second stage (Fig. 1):

$$Y = H_1 H_{\mathrm{dec}} U + NTF_D H_{\mathrm{dec}} Q_2, \qquad (1)$$

where H_1 is usually a delay factor, NTF_D is the digital replica of the first-stage noise transfer function, and H_{dec} is the transfer function of the decimation filter.

The reduced-sample-rate architecture requires that NTF_D be cancelled by the denominator of H_{dec}. In this case, (1) becomes

$$Y = H_1 H_{\mathrm{dec}} U + \mathrm{num}(H_{\mathrm{dec}}) Q_2, \qquad (2)$$
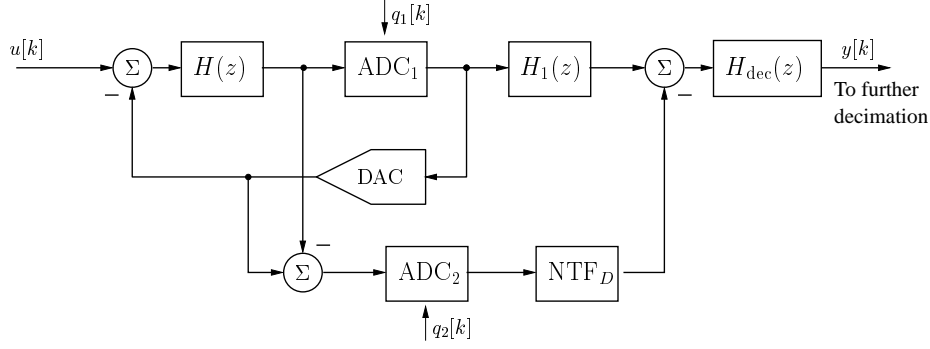
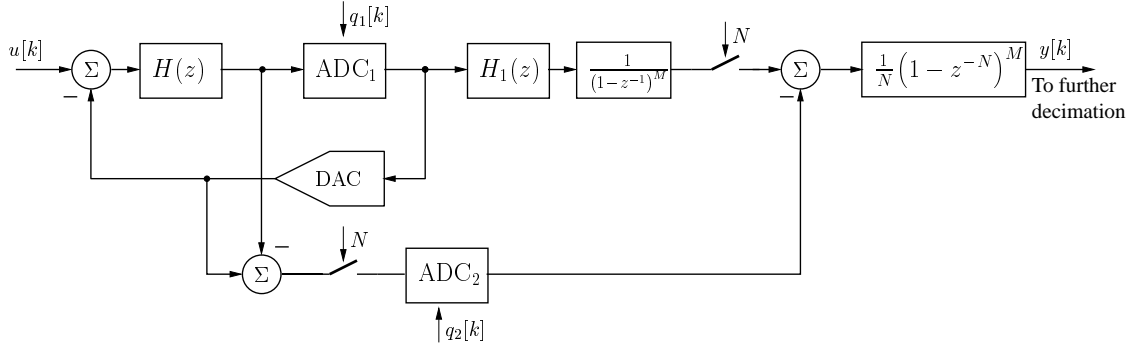Figure 1. The generalized Leslie-Singh architecture

Figure 2. The reduced-sample-rate architecture of [5]. M is the order of the modulator and the decimation filter.

where $\mathrm{num}(H_{\mathrm{dec}})$ denotes the numerator of the transfer function H_{dec}.

To maximize the SNR, the power of the inband noise has to be minimized. This can be done by re-locating the zeros of H_{dec} from $z = 1$. To keep the transfer function of the decimating filter close to 1 in the passband, the poles of H_{dec} has to be chosen so as to cancel the zeros around $f = 0$, and hence the NTF of the first stage has to be modified as well in order to be cancelled by the denominator of the decimation filter. This also minimizes the in-band noise of the first stage; however, ideally the noise from this stage will be cancelled by the second stage anyway.

Assuming that the decimation ratio of the first decimation stage is N, a second-order block of H_{dec} with the modified zeros and poles can be described as

$$H_{\mathrm{dec}}(z) = \frac{1 - 2(\cos N\alpha)z^{-N} + z^{-2N}}{1 - 2(\cos \alpha)z^{-1} + z^{-2}}, \qquad (3)$$

where α represents the angle of the complex conjugate zeros. If $\alpha = 0$, the expression becomes the classic sinc decimation filter. The function in (3) describes the transfer function of the so-called Rotated Sinc (RS) filter [8]. In our case, α should be optimized to minimize the inband noise power of in the output, i.e. to minimize

$$\int_0^{\frac{f_s}{2\,OSR}} |\mathrm{num}(H_{\mathrm{dec}})|^2 \, df. \qquad (4)$$

Using (3) and (4), it can be shown that the optimal α is

$$\alpha = \frac{1}{N} \cos^{-1} \left(\frac{\sin\left(\frac{\pi N}{OSR}\right)}{\frac{\pi N}{OSR}} \right). \qquad (5)$$

In a second-order structure one can achieve around 3.8 dB improvement in the SNR using this method, as compared to the traditional NTF and sinc filter. As the reduced-sample-rate structure has already 3 dB loss, the SNR in the proposed system can theoretically increase by about 0.8 dB.
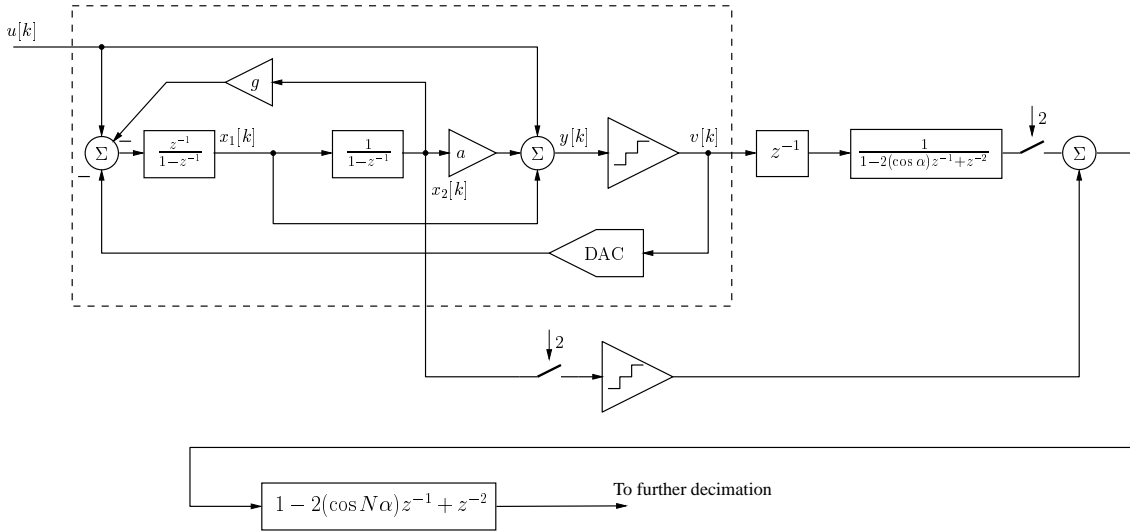
Figure 3. The simulated 2nd order system, with the modified first-stage in the dashed box ($OSR = 4$, $N = 2$, $\alpha = 0.44$, $g = 2 - 2\cos\alpha = 0.19$, $a = 1 - g = 0.81$). The resolutions of the two quantizers are 4 and 10 bits, respectively.

To cancel the digital NTF with the denominator of the decimation filter function, the first stage of the modulator has to be changed as well. To realize $NTF = 1 - 2\left(\cos\alpha\right)z^{-1} + z^{-2}$, the structure in the dashed box on Fig. 3 can be used [9], [4], where the coefficients g and a are $2 - 2\cos\alpha$ and $1 - g$, respectively. This topology has some other advantages as well, e.g. the output of the second integrator can be used to feed directly the second stage [4].

III. SIMULATION RESULTS

The verify the proposed technique, a second-order two-stage converter with an oversampling ratio of 4 has been simulated using MATLAB (Fig. 3). In this circuit, the second-stage DAC will be operated at only half of the oversampling rate.

Fig. 4 shows the transfer characteristic of the STF and the NTF of the whole system. The effects of the optimized zeros are clearly observable.

The output spectrum and the SNR after the first decimation stage are shown in Fig. 5. The reduced-sample-rate structure (Fig. 5(b), SNR = 98.61 dB) has a 3 dB loss compared to the original full-speed structure (Fig. 5(a), SNR = 101.62 dB). Using the proposed method (Fig. 5(c), SNR = 101.71 dB), the SNR is actually slightly improved compared to the original structure.

IV. CONCLUSION

A new design technique has been introduced which allows the use of a reduced-sample-rate second stage in a multi-stage $\Delta\Sigma$ structure without any loss in the SNR. A simple example was described to illustrate and verify the technique.

The method can be extended also for higher-order modulators, and then the sampling rate of the second stage will be even more significantly reduced, therefore lowering the speed and powe requirements. In addition, the SNR achieved by the proposed design is then better than that of the original full-speed structure.

It needs to be pointed out here that the described method is an optimization of the complete MASH structure, so it gives different results than the simple optimization of the zeros of a single-stage modulator [10], or the zeros of the decimation filter alone [8]. This method can be used for any two-stage structure even if the reduced-sample-rate structure is not used. In this case, one may use an $(N + 1)^{st}$-order decimation filter as suggested in [7].

The introduced topology increases somewhat the complexity of the first stage of the modulator and also that of the decimation filter. However, when the oversampling ratio is small (say, less than 8),
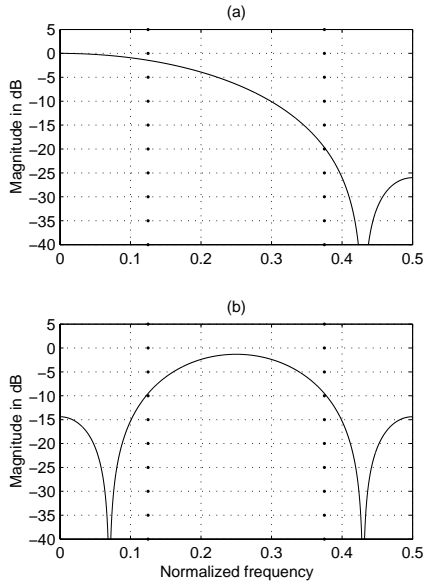
Figure 4. The STF and the NTF of the system. The two dotted lines show the boundary of the signal band and the band next to $f_s/2$ which folds back to the signal band after decimation.

Figure 5. The output spectra of the modulators. The dotted line shows the boundary of the signal band.
(a) 2nd order modulator, full-speed second stage, 3rd order decimator, $\mathrm{SNR} = 101.62$ dB; (b) reduced-sample-rate architecture, 2nd order decimation, $\mathrm{SNR} = 98.61$ dB; (c) proposed architecture, 2nd order decimation, $\mathrm{SNR} = 101.71$ dB.

the value of the extra feedback coefficient in the first stage is comparable to the other coefficients. There are also methods available which implement the decimation filter without a multiplier [11].

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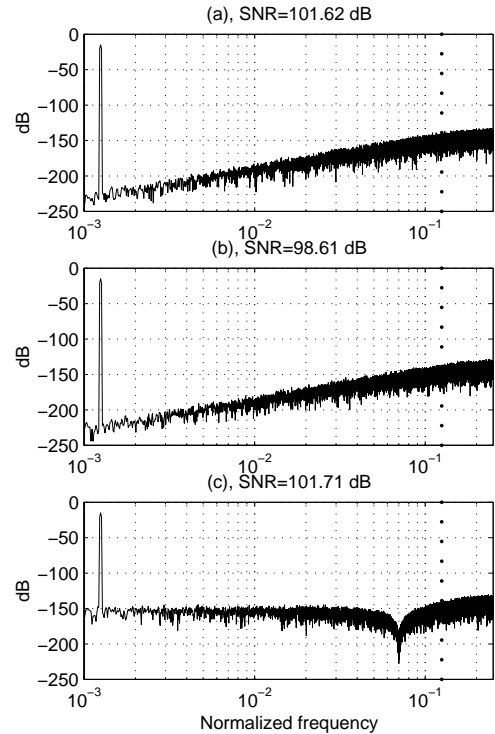[5] Wei Qin, Bo Hu, and Xieting Ling, "Sigma-delta ADC with reduced sample rate multibit quantizer," *IEEE Trans. on Circuits and Systems – II. Analog and Digital Signal Processing*, vol. 46, no. 6, pp. 824–828, June 1999.

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