IMPROVED NULL CANCELLATION IN A 6^{TH}-ORDER Σ-Δ MODULATOR REALIZED WITH TWO 3^{RD}-ORDER SECTIONS

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ABSTRACT

This paper presents an improved method to digitally correct for static, analog circuit imperfections in a two-stage, 6^{th} order, cascaded (6-3) sigma-delta modulator. By adding a digital correction term to the output of the digital noise cancellation filter, the first stage parasitic quantization noise due to finite amplifier gain and C-Ratio mismatches can be completely removed. A 6-3 modulator implemented as a fully differential switched-capacitor circuit, designed for an OSR of 16, has been fabricated in a 1.2μm double-poly n-well CMOS process. Improvements have been made in the null cancellation leading to approximately a 10 dB increase in SNDR over a range of signal amplitudes from 12 μVolts to 500 mV. A peak SNDR/SFDR of 87/100 dB for a 1 MHz sample rate and 84/93 dB for a 2.5 MHz sample rate have been achieved.

1. INTRODUCTION

There is a great deal of interest in extending the frequency range of sigma-delta modulators beyond the audio band. As the sampling rate of a system is increased, circuit imperfections progressively limit the effective dynamic range. Thus, the resolution can fall well below the theoretical maximum for a given modulator topology.

2. DOUBLE 3^{rd}-ORDER CASCADE MODULATOR

The modulator presented here obtains high resolution and wide bandwidth by cascading two identical 3^{rd} order sections. Each stage possesses a finite zero, yielding 2 nulls in the quantization noise spectrum . The use of ternary quantizers provides a greater dynamic range at a lower OSR without compromising stability. This network structure can provide 15 to 16 bit resolution for an OSR of 16 as long as the amplifier open loop gain exceeds 66-70 dB. A block diagram is shown in Fig. 1. The governing equations of this system are:

$$Y_1 = Xz^{-2} + N_1 \tfrac{1}{D_{10}} H_{13}(z) \quad (1)$$

$$Y_2 = [Y_1\ D_{10} - N_1]z^{-2} + N_2 \tfrac{1}{D_{20}} H_{23}(z) \quad (2)$$

where

$$H_{i3}(z) = (1-z^{-1})(1-z^{-1}[2-\delta_{6i}]+z^{-2}) \ \ for \ \ i = 1, 2 \quad (3)$$

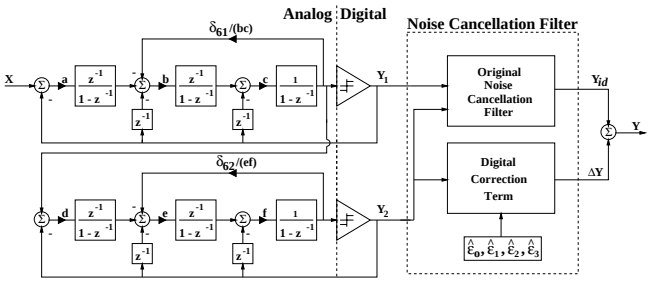

Fig. 1. Block diagram of the proposed double third-order cascade modulator.

The design procedure is similar to the techniques used to design any other higher order modulator. The techniques are fully described in [5, 6]. The two variables N_1 and N_2 denote the quantization noise of the first and second stage, respectively, while $D_{10} = a \cdot b \cdot c$ and $D_{20} = d \cdot e \cdot f$ represent the dc gain values of the two loop filters. In order to eliminate the first stage noise N_1, the following digital noise cancellation must be applied

$$Y_{id}(z) = \ Y_1\ z^{-2}\ [1 - H_{13}(z)] + Y_2\ \tfrac{1}{D_{10}}\ H_{13}(z) \quad (4)$$

The only remaining (quantization) noise contribution is the doubly third-order filtered quantization noise introduced by the second quantizer. By assuming two optimally positioned (l_2 norm) passband zeros (cf. [6]), a quantization voltage step of size V_{ref} and a sinusoidal input voltage with a swing of $g_0 V_{ref}$, the ideal signal to noise ratio (SNR) of this composite sixth-order modulator can be expressed as

$$SNR_{6-3} = \frac{1.2 \times 10^4}{\pi^{12}}\ {g_0}^2 {D_{10}}^2 {D_{20}}^2\ OSR^{13} \quad (5)$$

Inserting a practical value of $\frac{1}{8}$ for D_{10} and D_{20} and setting $g_0 = \frac{1}{2}$ yields SNRs between 95.5dB and 118.4dB if the oversampling ratio (OSR) varies from 16-24.

3. DIGITAL CORRECTION OF FINITE-GAIN AND C-RATIO MATCHING ERRORS

The forward Euler stray-insensitive switched-capacitor integrator is modified to include finite gain and C-Ratio matching errors. By assuming a finite amplifier open-loop gain

$A_0 = 1/\epsilon$ and a C-ratio value of a, the integrator z-domain transfer function can be written as

$$I(z) = \frac{a\ z^{-1}}{1 + \epsilon + a\ \epsilon - z^{-1}(1+\epsilon)} \quad (6)$$

If the ideal integrators are replaced by this model in the double third-order cascade structure an expression for a first order approximation of the parasitic noise contribution from the first stage is [4]

$$\Delta N_1 = N_1 \frac{1}{D_{10}}\ E(z) \quad (7)$$

where

$$\begin{aligned} E(z) &= \epsilon_3 H_{13}(z) + \epsilon_2 z^{-1}(1-z^{-1})^2 \\ &\quad -\epsilon_1 z^{-1}(1-z^{-1}) + \epsilon_0 z^{-2} \end{aligned} \quad (8)$$

and

$$\begin{aligned} \epsilon_0 &= \epsilon\ \delta_1\ a & \epsilon_1 &= \epsilon\ \delta_1[2+b+c] + \delta_1\epsilon_{m2} \\ \epsilon_2 &= \epsilon[a+b+c] & \epsilon_3 &= \epsilon[3+a+b+c] + \epsilon_{m1} \end{aligned} \quad (9)$$

Since the excess quantization noise caused by the first stage imperfections can be expressed with a relatively simple analytic expression, we can reconstruct an output signal which cancels the parasitic error contribution of the first stage quantization noise by digitally subtracting the excess noise ΔN_1 from Y_{id}. The corresponding additive correction term is [4]

$$\begin{aligned} \Delta Y(z) &= -\Delta N_1 z^{-2}[1 - H_{13}(z)] \\ &= -N_1 \frac{1}{D_{10}} z^{-2}[1 - H_{13}(z)]E(z) \end{aligned} \quad (10)$$

Since

$$Y_2 = Xz^{-4}D_{10} - N_1 z^{-2}[1 - H_{13}(z)] + N_2 \frac{1}{D_{20}} H_{23} \quad (11)$$

the digital correction term ΔY can be approximated by

$$\Delta Y \simeq Y_2\ \frac{1}{D_{10}}\ E(z) \quad (12)$$

The digitally corrected output $Y = Y_{id} + \Delta Y$ thus becomes

$$\begin{aligned} Y &= Xz^{-4}[1 + E(z)] \\ &\quad + N_2 \frac{1}{D_{10}D_{20}} H_{23}(z)[H_{13}(z) + E(z)] \end{aligned} \quad (13)$$

In the passband, the error function E(z) assumes very small values, thus the corrected output Y consists of an delayed version of the input signal X plus filtered quantization noise from the second stage. The parasitic error contribution of the first stage, which would have been the dominant noise source, has been algebraically canceled.

Notice that the estimates in Fig. 1, ϵ_i, $(i = 0, 1, 2, 3)$, are all dependent on the amplifier open loop gain. Furthermore, ϵ_1 and ϵ_3 are also dependent upon the C-Ratio matching errors of the coefficients and δ_1. Thus, a mismatch in D_{10} adds an additional error term ϵ_{m1} to the parameter ϵ_3 while a deviation of δ_1 adds the term $\delta_{61}\epsilon_{m2}$ to the value of ϵ_1 (ϵ_{mi} denotes the corresponding ratio mismatch). The selection of the values of $D_{10} = a{\cdot}b{\cdot}c$ and the first stage passband zero placing factor δ_{61} are the two most important parameters in this modulator network structure.

The performance of the digitally corrected noise canceler is sensitive to the estimate for δ_{61}. The term $\delta_{61}\epsilon_{m2}$ is proportional to δ_{61}. When using the digitally corrected noise-canceler the smaller null should be placed with the δ_{61} zero. This increase the in-band quantization noise for the un-corrected noise-canceler over that achieved when the higher frequency null is placed with δ_{61}.

4. CIRCUIT DESIGN

The prototype modulator, chip73, has been implemented as a fully differential switched-capacitor circuit in a a 1.2 μm double-poly n-well CMOS process. The major difference between chip73 and chip55 is in the null placement. Chip55 places the higher frequency null using stage 1 while chip73 places the lower frequency null using stage 1. The design value of each null leads to values for δ_{61} and δ_{62} of .01578 and .033203, respectively. The null placement is implemented in each loop by a single un-switched capacitive feedback element placed between the third amplifier output and the first amplifier input. The CMOS circuit has been designed for $\pm$2.5 V supplies and employs reference voltages of $\pm$1.54 V. Fig. 2 shows a micro-photograph of the prototype die. The entire modulator occupies a chip area of approximately 0.65 $mm \times 0.99\ mm$. Additional copies of the operational amplifiers used in the modulator have been made available with separate connections to estimate the amplifier gain of the integrators in the modulator circuit.

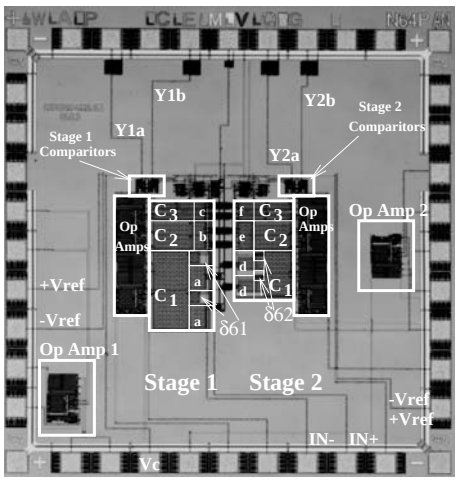

Fig. 2. Die micro-photograph of chip73.

The input capacitor has been chosen to be 3.53pF to match the approximate size of the input capacitor in chip55. The feedback capacitor is approximately 10-11 pF for both prototypes. All capacitors have been embedded in an n-well connected to analog ground to minimize substrate noise injection. The amplifiers have been realized using a fully-differential folded cascode structure complemented by a passive common-mode feedback circuit. The comparators have

been realized by a differential input stage followed by a resetable second gain stage that employs positive feedback to minimize slewing.

5. RESULTS

According to our measurements, the transconductance amplifiers provided a gain of approximately 650 while the C-Ratio mismatch of δ_{61} turned out to be 0.85 %.

The measured spectra for the uncorrected and digitally corrected noise cancelers are plotted in Fig.'s 3 and 4 for the 1 MHz sample rate and Fig. 5 for the 2.5 MHz sample rate. The FFT's in Fig.'s 3 and 5 are 2^{19}-points and averaged 4 times. The FFT in Fig. 4 is 2^{22}-points and is averaged 250 times. The 7-Term Blackman-Harris Window[7] was used for all spectral measurements including results where SNDR, SFDR and SFDR were computed.

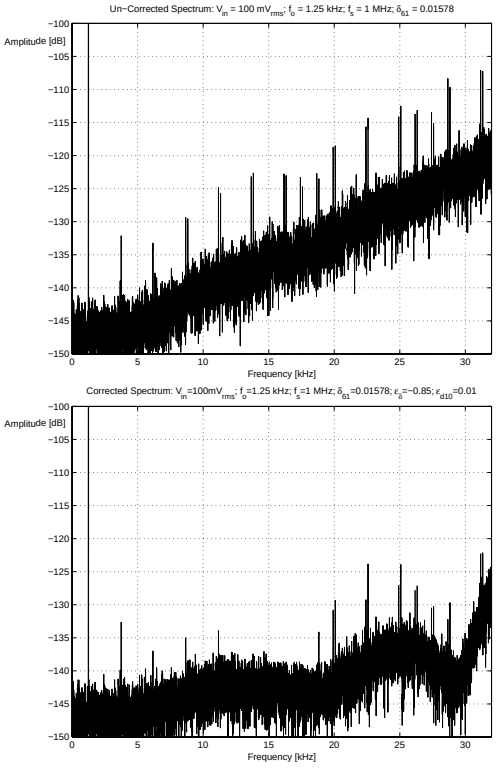

Fig. 3. Digitally corrected spectrum compared to an uncorrected spectrum for the 1 MHz sample rate.

In order to gain a better understanding of the noise structure, the chip73 measurement was carried out by adding 250 successive 2^{22} point FFTs. This spectrum measurement, displayed in Fig. 4, compares the uncorrected spectrum (top) to the digitally corrected spectrum (bottom). Unfortunately, the correction terms were found quickly and do not match those of Fig. 3 which we believe to be more accurate. This leads to higher in-band tones than what one would expect if the same correction parameters as those of Fig. 3 were used.

The spectra the 2.5 MHz sample rate are displayed in

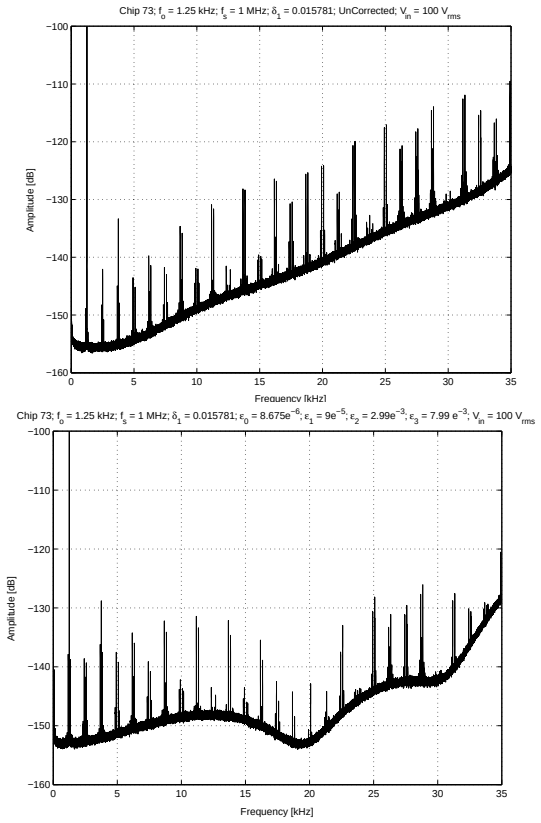

Fig. 4. Digitally corrected spectrum compared to an uncorrected spectrum for the 1 MHz sample rate using a higher resolution FFT.

Fig. 5 for the uncorrected and the digitally corrected noise-canceler. The input signal is a sine wave at 3.75 kHz with an amplitude of 100 mV_{rms}. There are more in-band tones for the 2.5 MHz digitally corrected noise canceler than for that observed in Fig. 3. This is most likely due to non-linear settling.

The SNDR vs. Input Signal Power was plotted in Fig. 6 for both the 1.0 MHz sample rate (top) and the 2.5 MHz sample rate (bottom). The input signal frequency was 1.25 kHz for the 1 MHz sample rate and 3.75 kHz for the 2.5 MHz sample rate. The FFT's for each signal level are 2^{19}-points in length averaged 4 times using the 7-Term Blackman-Harris Window[7]. The peak SNDR was 87 dB and 85 dB for the 1 MHz and 2.5 MHz sample rates respectively. We suspect that the reason for not obtaining more than 90 dB SNDR is due to limitations in settling and amplifier swing. The input capacitor could be reduced by a factor of 2 without significantly degrading the SNDR. Reducing the input capacitor size would effectively double the sample rate for the same given amplifier size. The first stage amplifier has a feedback capacitor which is four times the size of the 5 smaller amplifiers for the switched-capacitor filters which follow the first stage. The smaller amplifiers are designed for $\frac{1}{2}$ the slew rate of the first stage amplifier. Thus, reducing the capacitor sizing for stage1 will likely double the effective bandwidth.

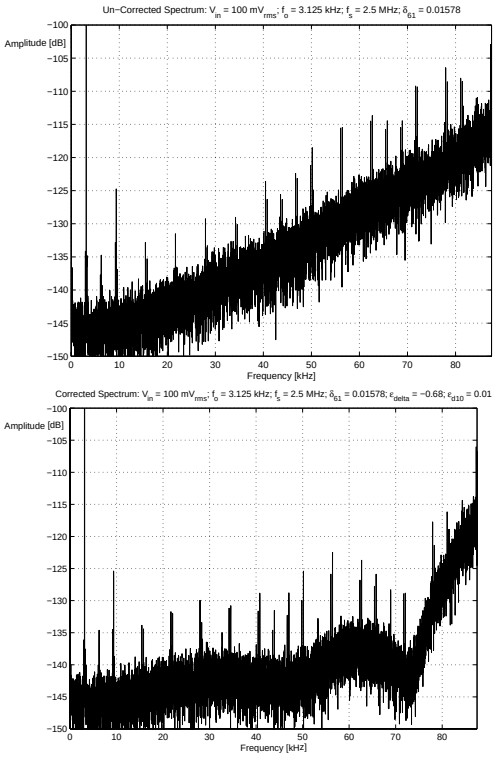

Fig. 5. Digitally corrected spectrum compared to an uncorrected spectrum for the 2.5 MHz sample rate.

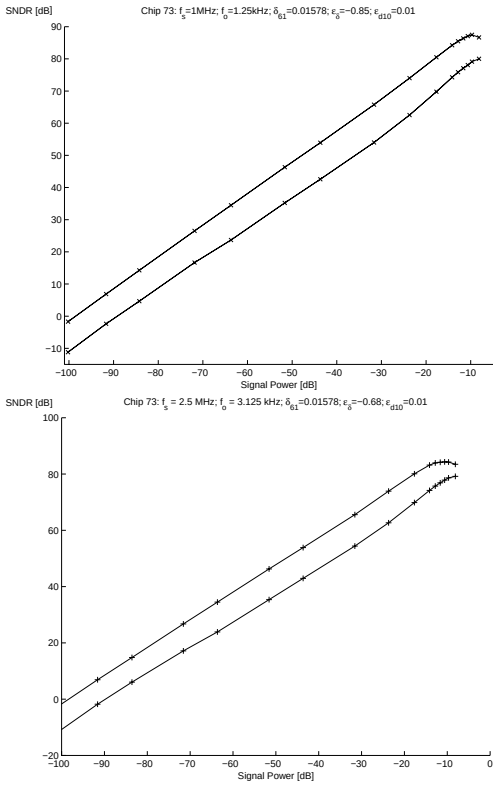

Fig. 6. SNDR vs. Input Signal Power.

The spectral measurements are summarized in Table 1.

Measurement	Chip73		Chip55	
dB	UnCorr	Corr	UnCorr	Corr
Max $SNDR$	79.1	87.5	81.5	84.2
Max $SFDR$	86.3	100.2	90.5	90.2
THD	-91.3	-95.3	-89.7	-89.7

6. CONCLUSIONS

A two-stage, 6^{th}-order modulator has been realized for relatively low gain by modifying the noise-canceler to compensate for static, parasitic errors due to analog circuit imperfections. The selection of the nulls are critical to the employment of adaptive noise-cancellation techniques. Since the parasitic errors due to matching are proportional to the null coefficient value correcting for the lower frequency null (e.g. placing the lower frequency null in stage1) dramatically improves the performance as seen with chip73 vs. the alternative (chip55).

7. REFERENCES

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