"Developing the Sigma-Delta A-D for precision DC&LF metrology"

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Keywords: *ADC, Sigma Delta, Metrology, Precision*

Summary & Introduction

The Sigma Delta (Σ-Δ) Analogue to Digital Conversion (ADC) technique is now very well established and reported in the literature. It is generally applied where long scale length, medium to high accuracy, conversion of DC and audio band AC is required and in particular, in Digital to Analogue guise, has probably achieved the widest use of any conversion technique through its application in CD players. It seems that whilst some applications require DC precision [1] most technical literature, eg [2], explains Sigma Delta Modulators using frequency domain techniques. However, traceability of precision metrology requires at least a good intuitive grasp of operation in the time domain.

The Digital Voltmeter (DVM) has become seen as a mundane workhorse instrument, so much so that it is forgotten just how well its Charge Balance ADC actually performs. Long scale length DVMs such as the Datron/Wavetek/Fluke 1281 and the HP/Agilent 3458 have been around for some 15 years now and it is interesting to translate their specifications into ADC parlance in order to see what needs to be done to match or better 15 year old designs! See Fig 1.

Figure 1: DVM Specifications in ADC Jargon

Specification	DVM spec. sheet	ADC "bit spec"
Nominal Resolution	8½ digits (±)	28 bits
Real (2σ) Resolution	7½ digits (±)	25 bits
Integral Non-linearity (INL)	.1ppm	23 bits
Differential Non-linearity	No spec. "perfect"	28 bits

One should note that these figures, on a like with like comparison, are nearly 2 orders better than the best merchant semiconductor chips. Traditional ways of specifying DVMs are also at variance with IEEE 1241 and in general specify peak errors rather than RMS.

The (Σ-Δ) ADC offers the potential to match these specifications at much higher speed and lower cost but the nature of the application of this class of measurement performance requires traceability and a high degree of confidence that the technique works for the specified range of measurement. To have confidence in an ADC for metrology one needs to understand how it performs in the sample or time domain. Since, in practice, it cannot be tested under all possible conditions one has to extrapolate from verifiable tests and to do so with justification requires knowledge of its operation. In other words, implied in "unbroken chains" of traceability is the assumption that the converter performs in an expected way. Charge balance is very easy to deal with in the time domain but Sigma Delta is certainly not and this may be what has limited its acceptance for precision work. This paper attempts to demonstrate operation in the time domain sufficiently well to give the required confidence.

DVMs and Charge Balance

It is helpful to review the basic Charge Balance technique so we can clearly see the similarities and differences to (Σ-Δ). The principle is seen in the 30+ year old "Dual Slope" method shown diagrammatically in Fig 2.

For Charge Balance and notation with capitals indicating "fixed" values and lower case variables we have:

$$I_{sig} \cdot T_s = I_{ref} \cdot t_r \quad \therefore I_{sig} = t_r \cdot \frac{T_s}{I_{ref}}$$

Or:

$$I_{sig} \cdot N_s \cdot t_c = I_{ref} \cdot n_r \cdot tc$$

$$\therefore I_{sig} = n_r \cdot \frac{N_s}{I_{ref}}$$

and N_s/I_{ref} is a constant, t_c cancels and n_r is the digital result.

The resolution of the device can be seen as the smallest quantum of charge that can be identified as a proportion of the total Full Scale input charge and this is clearly t_c/T_s where t_c is the clock period and T_s the integration period clearly needing very high clock rates or long integration periods for high resolution.

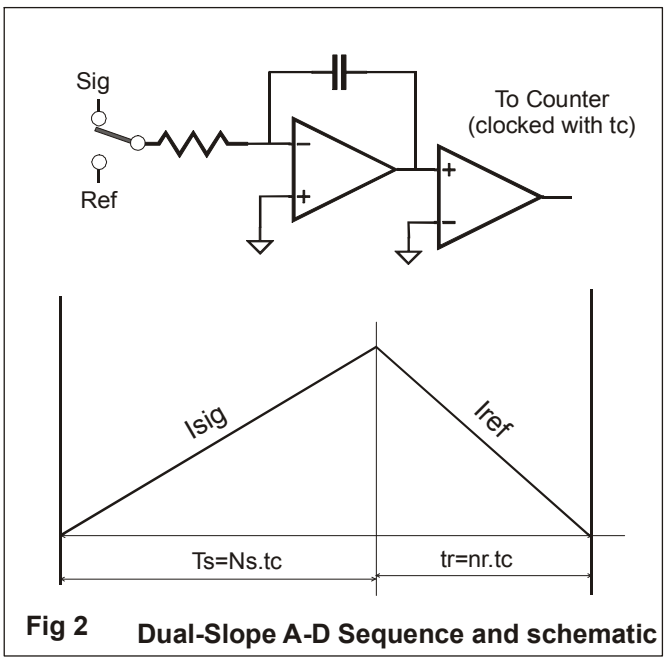


Fig 2 **Dual-Slope A-D Sequence and schematic**

The dual slope has been further developed in the instruments mentioned in the introduction in order to increase their digital sensitivity without greatly increasing clock rates. In order to do this it has been necessary to give the null detector an easier time!

In Fig 3 two key improvements are made. Firstly the integrator gain is increased by using a much smaller capacitor and since this would clearly cause saturation it is prevented by discharging the integrator cap regularly with "glugs" of known reference charge, ie reference current applied for integer numbers of clock periods. This process can be left running continuously and with sufficient time there will have been enough known reference pulses (of integer clock periods) to provide high resolution, however this could be a long time! The solution is to define a measurement period and at the end of the period any charge unbalance is forced to a final null with a smaller reference current (I_{ref}/K) so that one clock period now represents $1/K^{th}$ part of $I_{ref}.t_c$, effectively increasing the resolution by the factor K.

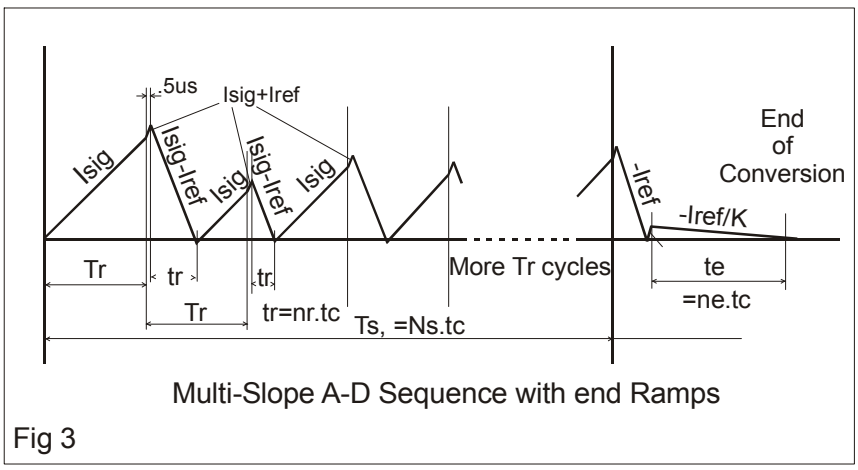
Using similar notation to the Dual slope case and ignoring the minor reference periods, which do not matter as long as charge balance is maintained and all reference periods "counted":

$$I_{sig} \cdot T_s = \sum I_{ref} \cdot t_r + \frac{I_{ref}}{K} \cdot t_e$$

and again tc cancels giving:

$$I_{sig} = \frac{I_{ref} \cdot n_e + \sum K \cdot I_{ref} \cdot n_r}{K \cdot N_s}$$

Which reveals a resolution of n/K. A variation used at lower accuracy in the HP/Agilent 34401 assumes null detector linearity and measures the charge unbalance with a fast successive approximation converter.



Multi-Slope A-D Sequence with end Ramps

Fig 3

Comparisons with (Σ-Δ), the Conundrum

At first sight the (Σ-Δ) converter appears similar to the charge balance converters and should therefore be subject to the same resolution rules.

For example in [1] a (Σ-Δ) ADC developed at CERN, Fig 4, takes independent readings at 1 per millisecond with Ref

clock periods timed with a 1 µsec clock. Since there is no amplitude modulation of the reference the resolution can only be 1 part in 1000 can't it? Well, real performance achieves 1ppm, some 3 orders better, so what is happening? At this point one can jump to the frequency domain [2] but trying to get a picture of this in the time domain we have to conclude that the implications (paras. 1 and 2) are actually quite staggering:

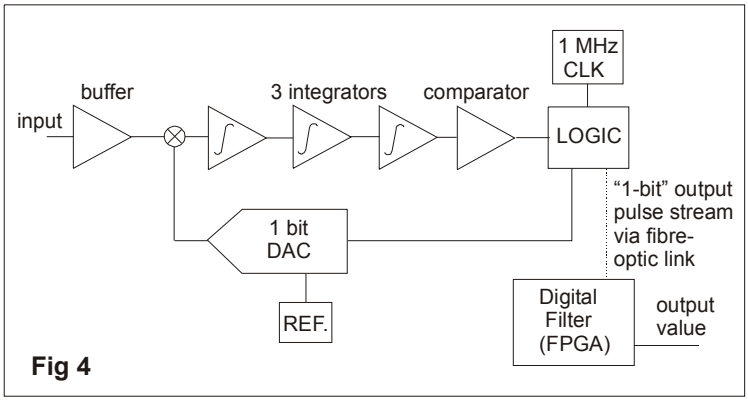


Fig 4

1. To achieve this performance the modulator (the integrator in charge balance) must be out of charge balance by up to 1000ppm when the reading taken appears to be of 1ppm resolution.

2. The digital filter (the counter in charge balance) "knows" how much the charge is out of balance from the history of the reference "glugs" of the previous 1000 clocks.

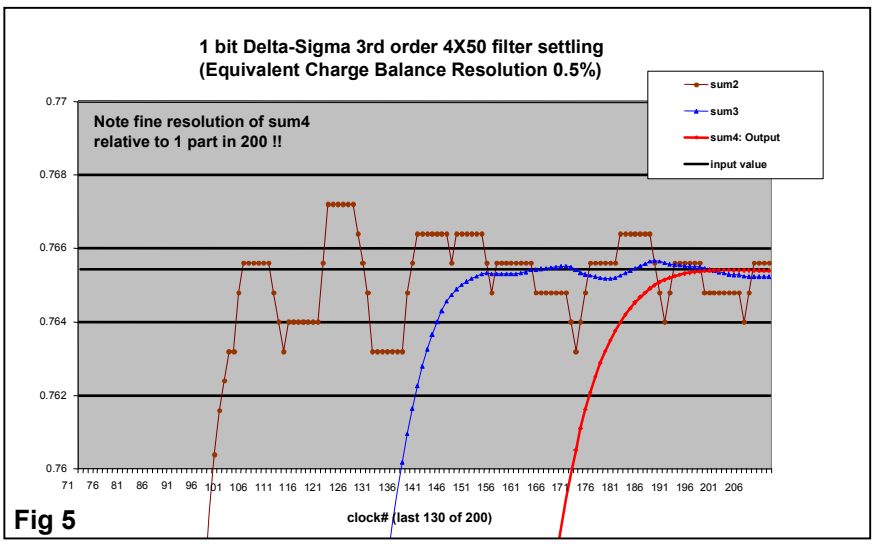


Fig 5

To an experienced "Charge Balance Expert" this is in the realms of magic!

We can demonstrate how this works in practice of course but in order to gain some confidence a simple simulator is highly informative. Fig 5 is the output from an Excel™ simulation of a third order modulator and sync4 filter with only 200 clocks which in charge balance would demonstrate only .5% resolution and it is clearly 2 orders better than this.

Combining Techniques

It is also clear from the 1 and 2 above that there must be opportunities to match the modulator and filter characteristics in a way that gives optimum response in terms of quantisation noise and number of clocks to settle. Those with fantastic mathematical abilities may be able to calculate those conditions but mortals can use imagination, instincts and the simulator. Beyond that we may consider the technique used in the multi-ramp charge balance converter where the reference amplitude is changed and this appears in various papers. The trick is to do it accurately.

DAC Reference Modulation.

Fig 6 shows a variation on Fig 4 where a low accuracy ADC is placed at the modulator output and its output is both fed to the digital filter and to a Digital to Analog Converter (DAC) to modulate the reference pulse amplitude. The ADC can be inaccurate because it is "inside the loop" but the DAC determines the full accuracy of the system which is a significant problem. However if it is achievable to metrology requirements the simulation shows very great advantages in performance, even from as little as 3 bits, because it allows the modulator loop gain to be significantly increased whilst maintaining stability. In a bipolar system it also substantially improves zero stability and noise because zero becomes the balance between +ve and -ve attenuated references rather than full amplitude references.

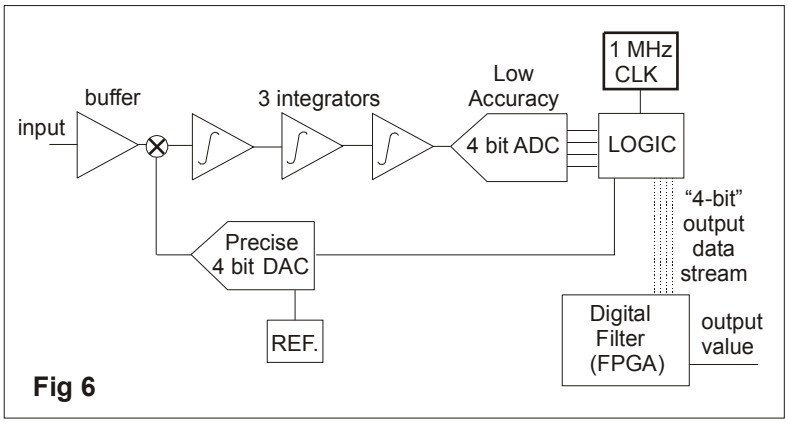


Fig 6

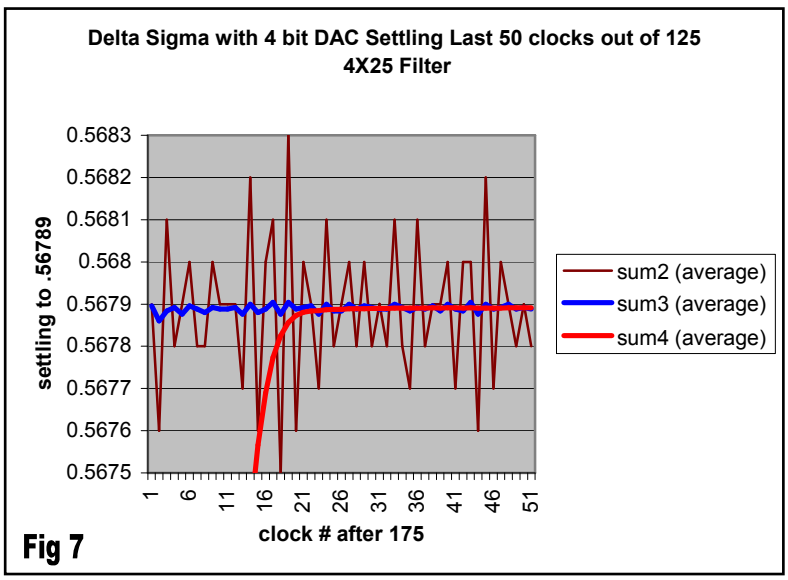


Fig 7

The circuit of Fig 6 is simulated in figure 7 exactly as shown in Fig 5 but in this case with the 4 bit DAC in the loop the final settling is to a few ppm in only 100 clocks.

To realise this potential needs all of the detailed design techniques and choice of component technology available to DVM designers and, as yet, not available in fully integrated technology. However, the combination of these together with the remarkable properties of (Σ-Δ) is capable of far exceeding Charge Balance at much higher speed and at lower cost.

The Ultimate DVM?

We have seen that placing a high accuracy, low resolution, DAC in the reference feedback path can give significant improvements in (Σ-Δ) performance. Such a device can be provided by Josephson Junction (JJ) Arrays and these can not only provide a "fundamentally" accurate reference at various Voltages but also the high speed, high accuracy switching required, [3],[4]. It seems quite feasible now, using JJs, to create a 28+ bit (Σ-Δ) ADC that settles within about 400 clocks and achieves 28 bit performance in noise, INL, DNL, and, with some self calibration, in stability. See Fig 8. Surely this must be the ultimate DVM in terms of DC and LF performance though many years of ongoing development inevitably will reduce size and cost whilst increasing speed.

Conclusions

The combination of DVM and (Σ-Δ) technology probably offers the ultimate measurement tool for DC and LF metrology and is sure to continue to be developed.

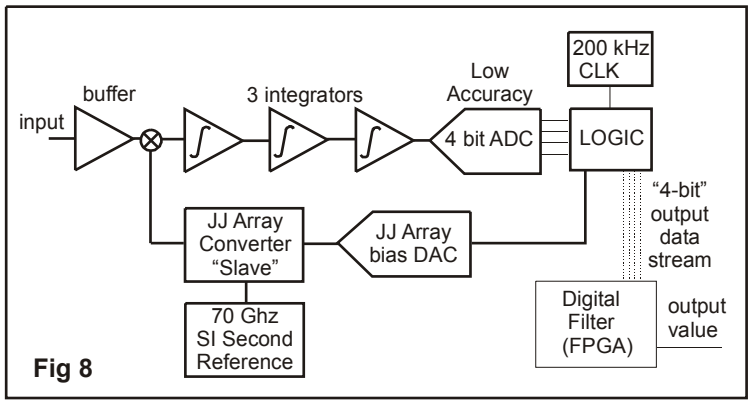


Fig 8

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