Superconductor ADCs based on processing of single flux quanta

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Summary

Superconductor ADCs exist and their performance is quickly approaching to those of the best semiconductor counterparts. Deep cooling could complicate a broad spreading of the still exotic superconductor technology. However, the technology is highly attractive for invention or at least numerical simulations of novel conversion schemes.

Introduction

The current place and future of superconductor electronics are very controversial. On one side you can find people demonstrating the fastest logic gate (T flip-flop) operating at over 750 GHz [1] and seriously developing a prototype of a superconductor microprocessor [2]. However, it is easy to find people who believe that superconductor electronics is a kind of science rather than real electronics. A practical resolution of this controversy is rather evident: there is no much sense to compete with the still fast progressing semiconductor digital industry. In other words, the superconductor digital electronics should wait until the predicted slow down of conventional digital electronics takes place.

It seems that a data conversion is much more favorable area for competition between semiconductors and superconductors. This is due to an intrinsic maturity of semiconductor analog-to-digital and digital-to-analog converters. This statement is well illustrated by a slow progress (one to two extra bits for 8 years) in converter performance [3]. Besides, superconductors could dramatically benefit from a natural and fundamentally accurate quantization effects that allow to eliminate many sources of conversion errors (such as an inaccuracy of resistive dividers).

Two quantum effects are potentially useful for data conversion:

Periodic dependence of properties on magnetic field (flash ADCs) [4, 5].

The most common circuit utilizing this effect is so-called two-junction Superconducting QUantum Interference Device (SQUID). It consists of two Josephson junctions (J1 and J2) connected by a superconducting strip with inductance L (Fig. 1a). (Each Josephson junction consists of two superconductor (Niobium) films connected by a small (10 micron^2) tunnel barrier with thickness about 20 A^o. Usually Josephson junction is shunted by a few Ohms resistor.)

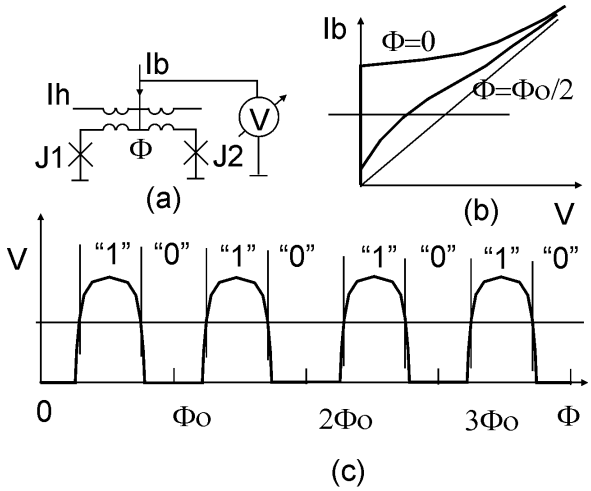

Fig. 1. Two-junction SQUID as a comparator with a multiple (periodic) thresholds.

The SQUID (see Fig. 1a) is biased by dc current Ib and magnetically via current Ih. Properties of the SQUID depend periodically on magnetic field H. However, the periodicity is fundamentally accurate if the period is measured in units of magnetic flux $\Phi = H \cdot S$ passing through the SQUID loop. (Here S is the area of the loop.). Figure 1b shows a typical voltage-current characteristics measured at zero magnetic field and at flux equals to a half of flux quantum:

$$\Phi_0 = h/2e \approx 2.07 \cdot 10^{-15} \text{Wb} \qquad (1)$$

Figure 1c shows a typical periodic dependence of output voltage V on magnetic flux Φ. at dc bias shown by the horizontal line in Fig. 1b. In fact, the circuit operates as a comparator with multiple and strongly periodical thresholds. It is possible to adjust the comparison level (the horizontal line in Fig. 1c) to get equal "lengths" of "0" and "1" areas. Similar comparators have been popular, say, 15 years ago mostly due to impressive hardware saving. However, suggested ADCs require a few similar comparators. These comparators have identical periods for

magnetic flux, but slightly different periods for corresponding currents Ih. In other words, unavoidable deviations in the wiring geometry from comparator to comparator spoils the quantum accuracy of the ADC.

Fundamental equivalence of Single Flux Quanta (SFQ)

Figure 2a shows more the core of advanced circuit that, in fact, performs as a delta modulator. (The dashed lines indicate that the circuit it only part of a much more complex circuitry.) Besides, inductance L is significantly larger, say, 50 pH to 100 pH. As a result the circuit operates by completely different way. In particular, junction J1 operates as a flux pump that injects received Single Flux Quanta into the loop (one per sampling period). This process shown by SFQ voltage pulses on upper trace in Fig 2b. The growth of magnetic flux leads to the proportional growth of induced current I. (middle trace in Fig. 2b) More exactly each injected fluxon increases current I on

$$\Delta I = \Phi_0 / L. \qquad (2)$$

The growth cannot continue infinitely: sooner or later

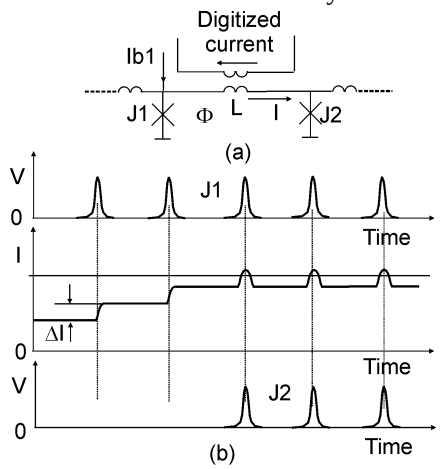

Fig. 2. Delta modulator. (a) Very simplified equivalent circuit, (b) Its operation.

current I reaches its threshold value (that is close to critical current of junction J2). When it happens the injected fluxons immediately escape from the loop through junction J2. (One can say that junction J2 operates as a current fuse.) Now let us note that the digitized current also take part in inducing of current I. It means that the digitized current is simply proportional to difference between the numbers of injected (Ninj) and released (Nrel) fluxons:

$$\text{Digitized current} \sim \Delta N = Ninj - Nrel \qquad (3)$$

Equation (3) shows that to recovery the digitized current one needs to count (or digitally integrates) fluxons released by junction J2. In other words, modulator itself behaves as a delta modulator. It is curious to note that junction J2 performs the functions of a comparator and a digital-to-analog converter.

Practical example (short version of a recent conference report [6], see also Ref. 7-10)

Chip design

Fig. 3 shows a 15-bit ADC chip utilizing so called phase modulation technique (a variety of delta modulation). The main focus of this design was to increase clock frequency up to 20 GHz. The ADC is equipped with programmable clock controller with externally selectable 1:128, 1:64, 1:32, 1:16 clock decimation ratios.

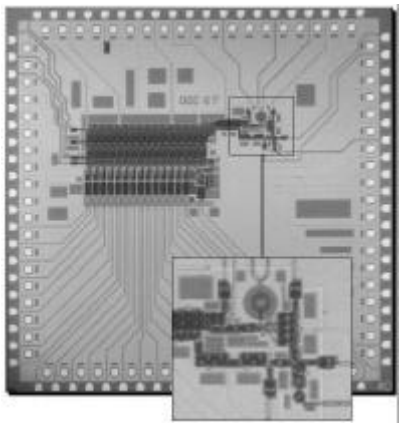

Fig. 3. Fifteen-bit ADC chip with a 2-channel synchronizer. The inset shows the ADC front-end (modulator). The 6,000-junction 1-cm^2 chip was fabricated using HYPRES' standard 1 kA/cm^2 process with a 3-μm minimum junction size.

Test results

Figure 4-6 shows the dynamic range (SINAD and SFDR) of the new and an old ADC chips for 10 MHz sinewave signal and for clock frequency of 11.2 GHz and 18.6 GHz.

Discussion

This 3-page paper is by no means a review of suggested or developed superconductor ADCs. We only tried to illustrate that superconductor converters really exist. The presented superconductor ADC chip (with on chip decimation filter) contains about 6,000 Josephson junctions and correctly operates at up to 19.6 GHz sampling frequency. To our knowledge, this is the world's fastest and most complex superconductive digital chip to date. We really believe that in a few years new superconductor ADC will outperform the best semiconductor counterparts.

However, superconductivity takes place at very low temperature, so the "cooling overhead" dramatically restricts the applications of superconductor ADCs to a few

niches, where the performance is highly important (metrology, modern digital communications ...)

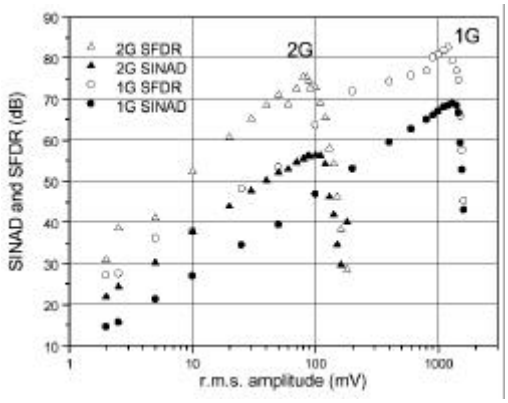

Fig. 4. Measured SINAD and SFDR for a 1G and a 2G ADC chips running at 175 MS/s (11.2 GHz clock with a 1:64 output decimation) and a 10 MHz input sinewave.

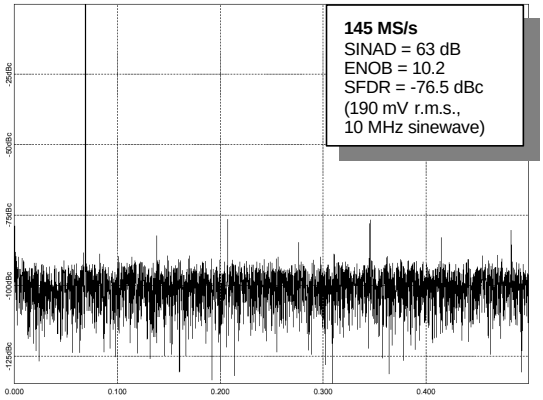

Fig. 5. Measurement of the ADC chip at 18.6 GHz clock using 16K-point FFT for a 10 MHz input sinewave at 145 MS/s data rate (1:128 on-chip decimation.

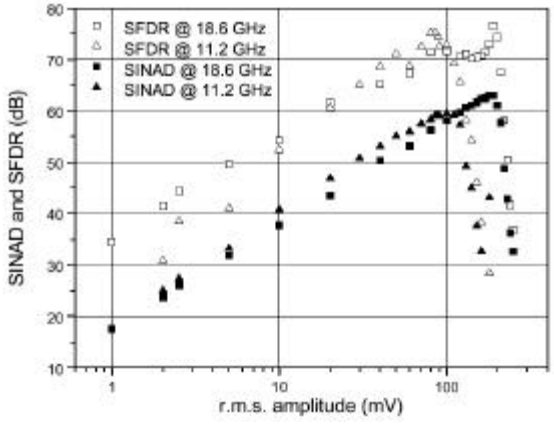

Fig. 6. Measured SINAD and SFDR for a 2G ADC chip running at 11.2 GHz and 18.6 GHz clock for a 10 MHz input sinewave. The selected 1:128 decimation ratio in the digital filter provides 87.5 MS/s and 145 MS/s output sample rate, respectively. But this area is a really "golden mine" for people who like to simulate (or invent) really novel ADCs.

Acknowledgment

The author likes to compensate the lack of corresponding references by thanks to some former and current collaborators: T. Filippov, A. Kirichenko, K. Likharev, O. Mukhanov, J. Przybysz, S. Rylov, and E. Wikborg.

References

[1] W. Chen, A.V. Rylyakov, V. Patel, J.E. Lukens, K.K. Likharev, "Rapid Single Flux Quantum T-flip flop operating up to 770 GHz", *IEEE Trans. on Appl. Supercond.*, 9 (2 Part 3): pp. 3212-15, , Jun. 1999

[2] M. Dorojevets, P. Bunyk, D. Zinoviev, "FLUX chip: Design of a 20-GHz 16-bit ultra pipelined RSFQ processor prototype based on 1.75-mu m LTS technology", *IEEE Trans. on Appl. Supercond.*, 11 (1 Part 1): pp. 326-32 Mar. 2001.

[3] R. Walden, "Analog-to-digital converter survey and analysis,", *IEEE J. Selec. Areas Comm.*, v. 17, pp. 539-50, 1999.

[4] P. Bradley, "A 6-bit Josephson flash A/D converter with GHz input bandwidth,", *IEEE Trans. Appl. Supercond.*, v. 3, pp. 2550-57, 1993.

[5] S.Rylov, V. Semenov, K. Likharev, "Josephson junction A/D converters using differential coding", *IEEE Trans.*" MAG 23, pp. 735-38, 1987.

[6] O. A. Mukhanov, I. V. Vernik, A. M. Kadin, D. Gupta, D. K. Brock, and I. Rochwarger, V. K. Semenov, T. V. Filippov, and Y. A. Polyakov, "High Resolution ADC Operation up to 19.6 GHz Clock", Ext. Abstract ISEC'01, pp. 309-10, Osaka, Japan, June 2001

[7] S. V. Rylov and R. P. Robertazzi, "Superconducting high-resolution A/D converter based on phase modulation and multichannel timing arbitration," *IEEE Trans. Appl. Supercond.*, vol. 9, pp. 2260-2263, June 1995.

[8] O. A. Mukhanov, V. K. Semenov, D. K. Brock, A. F. Kirichenko, W. Li, S. V. Rylov, J. M. Vogt, T. V. Filippov, Y. A. Polyakov, "Progress in the development of a superconductive high-resolution ADC," *Extended Abstracts of ISEC'99*, pp. 13-16, Berkeley, CA June 1999.

[9] O. A. Mukhanov, V. K. Semenov, W. Li, T. V. Filippov, D. Gupta, A. M. Kadin, D. K. Brock, A. F. Kirichenko, Yu. A. Polyakov, and I. V. Vernik, "A superconductor high-resolution ADC," *IEEE Trans. Appl. Supercond*., vol. 11, pp. 601-606, Mar. 2001.

[10] T. V. Filippov, S. Pflyuk, V. K. Semenov, and E. Wikborg, "Encoders and decimation filters for superconductor oversampling ADCs," *IEEE Trans. Appl. Supercond*., vol.11, pp. 545-549, Mar. 2001.