

MATHEMATICAL AND COMPUTER MODELS IN MULTI-PASS ADC DESIGN AND OPTIMISATION

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Abstract

The paper presents a mathematically grounded approach to the analysis and optimisation of multi-pass analogue-to-digital converters (MADCs) with the algorithmic forming the estimates of converted samples. The approach enables a comprehensive analysis of the converter work using a virtual model of MADC built on the basis of its mathematical model. This model is based on the extended optimal identification algorithms [2-4] adapted to the particularities of A/D conversion. The obtained sub-optimal algorithms take into account all main parameters of the internal auxiliary ADC and other analogue elements of MADC. The results of advanced simulations confirm a full agreement of theoretical and experimental evaluations, as well as efficiency of the proposed approach as a tool for MADC design support.

Keywords: multi-pass ADC, algorithmic conversion

1. Introduction

Recently, a lot of works appear concerning MADC design and applications (see e.g. bibliography in [1]). The main principle of MADC's functioning is iterative forming the estimates \hat{V}_k of the analogue sample V at the output of the "sample and hold" block.

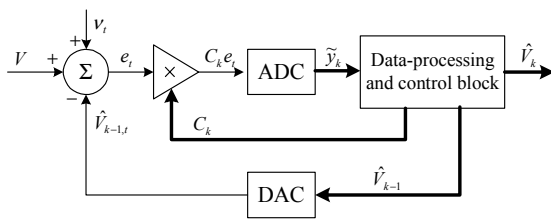


Fig. 1. Block diagram of multi-pass MADC

At each k -th ($k = 1, \dots, n$) cycle of conversion (see Fig. 1), the last calculated estimate \hat{V}_{k-1} is routed, via feedback with N_{DAC} -bit digital-to-analogue converter (DAC), to the input of the subtracting block. Residual signal $e_t = V - \hat{V}_{k-1,t} + v_t$ (lower indices in $\hat{V}_{k-1,t}$ denote the time-continuous signal corresponding to the digital estimate \hat{V}_{k-1}) is routed to the switched gain C_k amplifier. Variable v_t describes a summary external and

feedback circuit noise. The amplified residual signal $\tilde{y}_t = C_t e_t + \xi_t^{(1)}$ ($\xi_t^{(1)}$ denotes the internal noise of the amplifier) is converted by the internal auxiliary low-resolution N_{ADC} -bit ADC. Each subsequent estimate \hat{V}_k is calculated in data-processing block using the value \tilde{y}_k and previous estimate \hat{V}_{k-1} calculated on the basis of observations $\tilde{y}_1, \dots, \tilde{y}_{k-1}$, and the cycle repeats.

The multi-cycle conversion makes actual application of data-processing algorithms for the noise suppression. Unfortunately, any direct calculations and derivation of algorithms of this kind for MADC are impossible due to the step-wise form of characteristic of the internal ADC (see Fig. 2, the gain of amplifier is included):

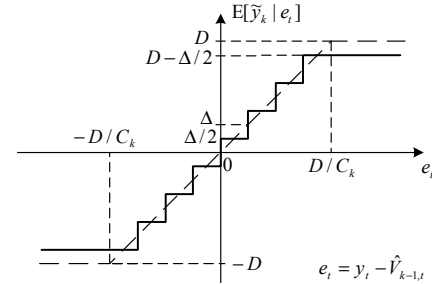


Fig. 2. Characteristic of internal conversion block

Nevertheless, this difficulty can be omitted by employing the properly modified extended algorithms [2-4]. These algorithms have a number of important properties. Namely, they ensure concurrent iterative optimal estimation of input signals under simultaneous adaptive adjustment of the sensor parameters to the conditions of measurement. This significantly improves the accuracy of estimates, extends the measurement range and shortens the time of measurement [2-5]. These algorithms take into account the always-limited input range of the sensors and adjust them in the way ruling out their possible saturation at each cycle of conversion.

These properties of extended algorithms correspond well to the particularities of MADC's work. The only obstacle to their direct application to MADC is the step-wise form of the internal ADC characteristic. To solve this problem, we suggest that the extended algorithms, optimal for the strictly linear working range of the sensor characteristic (dashed line in Fig. 2), should preserve close to optimal (sub-optimal) properties being

applied to MADC with a step-wise characteristic (at least for a not too large Δ). This suggestion was analysed in [6,7]. The performed simulations confirmed the expected effects.

The results of analysis show that direct theoretical evaluation of the speed and quality of conversion can be done only for a small number of initial cycles of conversion [7]. In many cases it can be insufficient for engineering applications. Then, necessary information can be delivered by modelling. The results of simulations show high agreement of theoretic and measured characteristics of MADC. This gives us reasons to assume that a virtual model of algorithmic MADCs may serve as a convenient and reliable tool for comprehensive analysis of their properties and characteristics at the initial stage of design. This model, corresponding testing software and the results of experiments are discussed below.

2. Mathematical model of MADC

As a sufficiently good approximation of the step-wise characteristic in Fig. 1, we use the piece-wise linear model [2-4]:

$$\tilde{y}_k = \begin{cases} C_k e_t + \xi_t, & \text{for } |e_t| \leq D/C_k, \\ D \operatorname{sgn}(e_t) + \xi_t, & \text{for } |e_t| > D/C_k, \end{cases} \quad (1)$$

where D describes the limited input range $[-D, D]$ and $e_t = V - \hat{V}_{k-1,t} + v_t$ is the residual signal at the k -th cycle of conversion and the noise v_t is a zero-mean white Gaussian noise with the variance σ_v^2 . Unlike in [2-4], noise ξ_t in (1) is a quantisation noise of the internal ADC. Then its variance is determined as follows:

$$\sigma_\xi^2 = \Delta_{ADC}^2 / 12 = D^2 \cdot 2^{-2N_{ADC}} / 3, \quad (2)$$

where $\Delta_{ADC} = D/(2^{N_{ADC}-1})$ is the quantisation step.

Algorithms for the systems with input blocks described by (2) can be derived only if possibility of saturation at each cycle of conversion is excluded. This can be done using simple and clear *fitting condition* [2-4]:

$$\Pr[|e_k| \leq D/C_k \mid \tilde{y}_1^{k-1}] \geq 1 - \mu. \quad (3)$$

For each $k = 1, 2, \dots$ and corresponding estimate \hat{V}_{k-1} , this condition determines "acceptable" values of C_k , for which the amplified residual sample e_k will pass the ADC without saturation with probability not less than a given (confidence) level $1 - \mu$. For a small value of μ (of the order of $10^{-5} \div 10^{-15}$) and C_k satisfying (3), abnormal errors will be practically eliminated, and model (1) can be replaced by the linear model with the same parameters. In this case, derivation of algorithms can be performed using conventional linear theory of

optimal identification and filtering. According to the results of works [2-4], in considered case, the extended algorithm for optimal estimates \hat{V}_k calculation has the form:

$$\hat{V}_k = \hat{V}_{k-1} + \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2} \tilde{y}_k, \quad (4)$$

$$P_k = \frac{(\sigma_\xi^2 + C_k^2 \sigma_v^2) P_{k-1}}{\sigma_\xi^2 + C_k^2 (\sigma_v^2 + P_{k-1})}, \quad (5)$$

$$C_k = D / \alpha \sqrt{\sigma_v^2 + P_{k-1}}, \quad (6)$$

where $P_k = E[(\hat{V}_k - V)^2]$ is the variance of estimation errors. Initial values $\hat{V}_0 = V_0$ and $P_0 = \sigma_v^2$ are the mean value and variance of the sample V at the "sample and hold" block output. Constant α satisfies the equation:

$$\frac{1}{\sqrt{2\pi}} \int_0^\alpha \exp(-x^2/2) dx = \frac{1-\mu}{2}. \quad (7)$$

Formulas (6),(7) determine, at each cycle, the greatest acceptable gain C_k satisfying (3). For these values the variance P_k of estimates \hat{V}_k at the initial cycles of conversion ($k = 1, 2, \dots$) diminishes *exponentially* [2-7]:

$$P_k = \sigma_v^2 (1 + Q^2)^{-k}; \quad Q^2 = \frac{C_k^2 E[e_t^2]}{\sigma_\xi^2} = \left(\frac{D}{\alpha \sigma_\xi} \right)^2. \quad (8)$$

When P_k reaches the value of the order of $\sigma_v^2 (1 + Q^2)$, exponentially fast diminution of estimation errors slows down and takes the hyperbolic form.

Algorithm (4)-(7) is optimal for the "smoothed" model (1) of the internal converter and Gaussian internal noise ξ_t . The sub-optimal algorithm for the "real" converter as in Fig. 2 has the same form, but with the variance σ_ξ^2 determined by formula (2). In this case, at the initial cycles of conversion, the decibel mean square error (MSE) of conversion and resolution N_{ADC} of MADC depend on k as follows:

$$\begin{aligned} \text{MSE}(k) &= 10 \log_{10} \left(\frac{P_k}{\sigma_v^2} \right) = \\ &= -10k \log_{10} \left(1 + \frac{3}{\alpha^2} 2^{2N_{ADC}} \right) [\text{dB}], \end{aligned} \quad (9)$$

$$\begin{aligned} N_{MADC}(k) &= \frac{1}{2} \log_2 \left(\frac{\sigma_v^2}{P_k} \right) = \\ &= \frac{k}{2} \log_2 \left(1 + \frac{3}{\alpha^2} 2^{2N_{ADC}} \right) [\text{bit}]. \end{aligned} \quad (10)$$

Formula (10) also describes the Shannon's measure of information about sample V delivered by observations $\{\tilde{y}_1, \dots, \tilde{y}_k\}$: $I(V, \tilde{y}_1^k) = H(V) - H(V \mid \tilde{y}_1^k)$, where $H(V)$ and $H(V \mid \tilde{y}_1^k)$ are the prior and posterior entropies of the samples respectively [8].

3. Computer analysis of algorithmic multi-pass ADC

Using a full mathematical model of MADC with algorithmic estimates forming, we can build simple re-configurable and universal research software for analysis, comparison and optimisation of different versions of MADC and other types of ADC. This software (in package form), consists of three modules: generator of testing signals and noises, a full model of algorithmic MADC (as in Fig. 1) with algorithm (4)-(7), and data-processing and controlling blocks connected to monitor.

The particular feature of this package is that the full MADC model used is optimal or close to optimal. It means this model ensures the fastest rate of conversion among the other versions of MADC constructed using the same elements and operating under given conditions. For this reason, it may serve as a standard for evaluation of the efficiency of simplified technical solutions. Being easily re-configurable to different conditions and requirements of experiment, this package can be used for selection of MADCs' configuration and parameters, which are most appropriate for the conversion of the given class of the input signals. It can be used for the fast and comprehensive analysis of MADC's parameters, internal and external noises and influence of technological errors on the quality of conversion.

Traditionally, virtual modelling is used as design support in the cases of lack of formal tools for the designed systems quality evaluation and analysis. In our case, main employed model of algorithmic MADC is built on an adequate and mathematically based presentation of the analogue and digital components of the converter. The modelling serves here as a support of analytical investigations, when direct calculation, evaluation and analysis of required characteristics of converters are impossible.

To illustrate the possibilities of the approach, we present below the results of different experiments clarifying details of algorithmic MADC functioning.

As the testing signals, sequences of $M = 1000$ samples $\{V^{(1)}, \dots, V^{(M)}\}$ were used. The samples were generated as independent, normally distributed random values with the variance σ_V^2 and mean value V_0 . Each sample was converted using n -pass MADC. The quality of conversion was estimated using following measures calculated on the basis of estimates $\hat{V}_k^{(m)}$ obtained at the k -th cycle of conversion of each sample $V^{(m)}$:

$$\text{EMSE}(k) = 10 \log_{10} \left\{ \frac{1}{\sigma_V^2 M} \sum_{m=1}^M [\hat{V}_k^{(m)} - V^{(m)}]^2 \right\} \text{ [dB]}, \quad (11)$$

$$N_{MADC}(k) = -\frac{1}{2} \log_2 \left\{ \frac{1}{\sigma_V^2 M} \sum_{m=1}^M [\hat{V}_k^{(m)} - V^{(m)}]^2 \right\} = \quad (12)$$

$$= -0.1661 \text{EMSE}(k) \text{ [bit]}.$$

These measures correspond directly to (9), (10) and were calculated by averaging the sets of conversion errors $\{\hat{V}_k^{(1)} - V^{(1)}, \dots, \hat{V}_k^{(M)} - V^{(M)}\}$ in the k -th iteration of conversion for each sample $V^{(m)}$.

Fig. 3a-b presents the plots for $\text{EMSE}(k)$ (continuous lines, from top to bottom) and for $N_{MADC}(k)$ obtained for different resolution of the internal ADC $N_{ADC} = 1, \dots, 8$. The parameters of the testing signal, amplifier and ADC had the values: $\hat{V}_0 = 0$, $P_0 = 2.56$, $D = 1$, $\alpha = 5$, $\mu = 10^7$. The value of variance σ_V^2 was taken as referring to the least significant bit (LSB) of DAC in the feedback, and calculated similarly to variance (2) under $N_{DAC} = 16$, $D_{DAC} = 8$. As follows from the plots, for each N_{ADC} diminution of $\text{EMSE}(k)$ and initial growth of resolution $N_{MADC}(k)$ are linear, and the slope of corresponding plots is equal to the ones determined by (9),(10). The dashed lines in Fig. 3a-b present the theoretical values of $\text{EMSE}(k)$ and $N_{MADC}(k)$. For $N_{ADC} \geq 3$ the measured and theoretical plots are practically identical. For $N_{ADC} \geq 8$ all the plots have similar form. Values $D_{DAC} = 8$ and $\sigma_V = 1.6$ were chosen to obtain the gain $C_1 = 1/8$ in the first iteration, which enables us to compare the final resolution of algorithmic two-pass MADC and two-pass 13-bit converter HP3561 described in [9]. The main parameters of this converter are: $N_{ADC} = 8$, $N_{DAC} = 13$, $C_1 = 1/8$, $C_2 = 4$. The experimental plots of resolution (12) for two-pass MADC and HP 3561 are shown in Fig. 3c. After the second iteration, the resolution of MADC (continuous line) is about 1.5 bit greater than the resolution of HP 3561 (dashed line). Direct calculation of resolution according to the formula (10) gives the values: $N_{MADC}(2) = 12.94$, $N_{HP}(2) = 11.47$. This shows the existence of unemployed resources in HP 3561, which could be utilized by application of sub-optimal algorithm (4)-(7).

Fig. 3d presents changes of the MADC resolution depending on the improper application of the converter to signals with variance σ_V^2 greater than the assumed value $P_0 = 2.56$. For $\sigma_V^2 = 1; 1.5; 2; 2.5; 3 \cdot P_0$ corresponding resolution diminishes due to appearance of rare and more frequent for the greater σ_V^2 abnormal errors.

The plots in Fig. 3e show the dependence of MADC resolution on the feedback noise v_f , in this case - on the finite resolution of DAC. The plots correspond (from bottom to top) to $N_{DAC} = 12, 13, 14, 15, 16$ bit. The last Fig. 3f illustrates the work of algorithmic MADC for $N_{ADC} = 4, 6, 8$ bit. One can see that the 13-bit resolution can be achieved for $N_{ADC} = 8$ in two iterations, for $N_{ADC} = 6$ in three, and for $N_{ADC} = 4$ in five iterations.

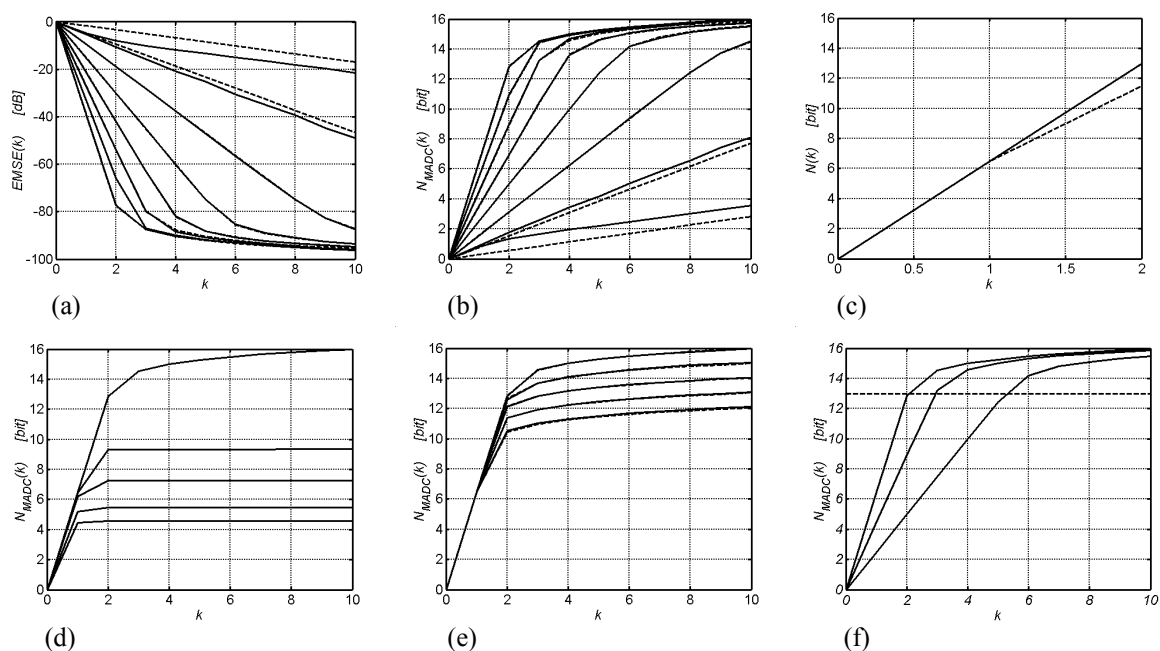


Fig. 3. Effective resolution of MADC as a function of iterations number for different simulation conditions

4. Conclusions

The results presented in the paper show that both proposed mathematical and mathematically based virtual models of algorithmic MADC can be used as efficient tools in MADC design and optimisation. An important feature of the approach is the complex consideration of the “hardware and software” functioning. The results of such a consideration enable us to design converters with close to the highest, under given conditions, rate and accuracy of conversion.

The results of advanced simulations confirm a high degree of coincidence of theoretical and experimental evaluations. This means that the mathematically based virtual model of algorithmic MADC, considered in the paper, can be used by engineers for an accurate, simple and fast qualitative and numerical analysis of the details of their work. Moreover, simulations performed using this model may answer more complex questions than the analytical investigation is able to. This can be done much faster, does not require special training and may significantly simplify and optimise the MADC design.

References

[1] F. Maloberti, “High-speed data converters for communication systems”, *IEEE Circuit and Systems Magazine*, vol.1, No.1, pp. 18-36, Jan. 2001.
 [2] A.A. Platonov, “Optimal adaptive system for random values estimating under limitations on the dynamic range of the registering devices”, *Inter*

High-School Scient. Proc. "Woprosy peredachi i preobrazowania informacii", RRTI, Riazan', pp. 35-40, 1986, (in Russian).

[3] A.A. Platonov, “Basic theoretical principles for design of analog-digital measurements systems with adaptively controlled sensors”, *Proc. IMEKO XIII World Congress*, Torino, Italy, vol.2, pp. 1025-1031, Sept. 1994.
 [4] A.A. Platonov, “Optimal identification of regression-type processes under adaptively controlled observations”, *IEEE Trans. Signal Processing*, vol. 42, No. 9, pp. 2280-2291, Sept. 1994.
 [5] A.A. Platonov, J. Szabatın, “Analog-digital systems for adaptive measurements and parameter estimation of noisy processes”, *IEEE Trans. Instrum. Meas.*, vol.45, No.1, pp. 60-69, Feb. 1996.
 [6] K. Jędrzejewski, A.A. Platonov, “A new approach to optimisation of adaptive ADC with multi-pass residual compensation”, *Proc. Polish-Czech-Hungarian Workshop on Circuits Theory, Signal Processing and Telecommunication Networks*, Budapest, Hungary, pp. 11-18, Sept. 2001.
 [7] A.A. Platonov, J. Jasnos, “Improvement of resolution and speed of conversion in multi-pass A/D converters with microprocessors”, *Proc. MWiPPP'-2001 Conference*, Gliwice, Poland, Nov. 2001.
 [8] R.G. Gallager, *Information Theory and Reliable Communication*, New York, Wiley, 1968.
 [9] J.S. Epstein, G.R. Engel, D.R. Hiller, G.L. Purdy, B.C. Hoog, E.J. Wicklund, “Hardware design for dynamic signal analyzer”. *Hewlett Packard Journal*, pp. 12-17, Dec. 1984.