Real-time Correction of DC Offset of Low-cost Audio Codecs in Acoustic Digital Lock-in Amplifiers

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SUMMARY

In design of the DSP for acoustic applications it is appropriate to integrate a low-cost audio codec [1] into their structure. Audio stereo codecs are able to achieve a high resolution of measurement on low frequencies of the input signal. But audio codecs are able to digitalize only signals of the acoustic origin, it means the signal without the DC part of frequency spectrum. In the majority of available DSP there are 2 independent AD converters and also 2 DA converters. But most of audio codecs create the DC offset during the conversion to the digital form, it means 0V voltage amplitude of input signal doesn't correspond to 0_{HEX} in hexadecimal form of output digital word. The solution how to achieve the required parameters with these low-cost audio codecs is founded in this project.

KEYWORDS

audio codec, correction of DC offset, digital signal processing

STATEMENT Introduction

The audio codec built in DSP could be easily used for construction of digital lock-in amplifiers working in audio frequencies band. Similarly the DA converters could produce the auxiliary output signals. Simple interface structure and behavioural model is the important advantage of these ICs too. Functional diagram of the digital of lock-in amplifier based on DSP is shown in fig. 1.



Fig. 1: Lock-in amplifier

Theoretical analysis

As it has been already mentioned the main problem of audio codecs is their output DC offset. Due to the special internal structure of ADC channel components, such as input approximation digital filter, the output signal in digital form doesn't correspond exactly to the input analog DC amplitude. It means, the output digital value, that equals to 0_{HEX} , doesn't correspond to the input signal amplitude 0V.

The solution of this problem is available by two different ways. The first way is based on the finding out the DC offset of ADC before a measurement and the subtraction the measured DC offset from the analyzed signal amplitude. This method is shown in Fig. 2.



Fig. 2: "Classical" IC design to eliminate DCoffset based error

The correction of shown method is described by the following equation:

$$u_{OUT-CRTD}(n) = \frac{1}{N} \sum_{n=1}^{N} \left[\left(u_{sig}(n) - U_{sig-DC} \right)^{*} \left(u_{ref}(n) - U_{ref-DC} \right) \right]$$

It means, that the correction value has to be archived in the non-volatile memory. The more precise solution is based on premeasurement calibration. This solution doesn't require the non-volatile memory but the calibration before every measurement is slow and difficult process. Then the accuracy of measurement depends also on the precision of calibration procedure.

The second way is based on the approach described bellow. Because the analyzed signal contains only AC part of frequency spectrum, we can suppose that the mean value of analyzed and reference signal are equal to zero. The principle of the method is described by the following equations:

$$\begin{aligned} u_{sig}(n) &= u_{sig-AC} + U_{sig-DC} \\ u_{ref}(n) &= u_{ref-AC} + U_{ref-DC} \\ \frac{1}{N} \sum_{n=1}^{N} (u_{ref-AC}(n)) &= 0 \\ \frac{1}{N} \sum_{n=1}^{N} (u_{sig-AC}(n)) &= 0 \end{aligned}$$

$$\begin{split} u_{OUT}(n) &= \frac{1}{N} \sum_{n=1}^{N} \left[u_{ref}(n)^* u_{sig}(n) \right] \\ u_{OUT}(n) &= \frac{1}{N} \sum_{n=1}^{N} \left[\begin{pmatrix} u_{sig-AC}(n)^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-DC}^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-AC}(n)^* u_{ref-DC} \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-AC}(n)^* u_{ref-DC} \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-DC}^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \frac{u_{sig-DC}}{N} \sum_{n=1}^{N} \left(u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-AC}(n)^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = \frac{1}{N} \sum_{n=1}^{N} \left[\begin{pmatrix} u_{sig-AC}(n)^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = \frac{1}{N} \sum_{n=1}^{N} \left[\begin{pmatrix} u_{sig-AC}(n)^* u_{ref-AC}(n) \end{pmatrix}_{+} \\ &+ \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT-CTRD}(n) + \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT-CTRD}(n) + \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT-CTRD}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT-CTRD}(n) + \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) \\ &u_{OUT}(n) = u_{OUT}(n) - \begin{pmatrix} u_{sig-DC}^* u_{ref-DC} \end{pmatrix}_{n=1} \\ &u_{OUT}(n) \\ &u_{OUT}(n)$$

$$U_{sig-DC} = \frac{1}{N} \sum_{n=1}^{N} (u_{sig}(n))$$
$$U_{ref-DC} = \frac{1}{N} \sum_{n=1}^{N} (u_{ref}(n))$$

$$u_{OUT-CRTD}(n) = u_{OUT}(n) - (U_{sig-DC} * U_{ref-DC})$$
$$u_{OUT-CRTD}(n) = u_{OUT}(n) - \frac{1}{N^2} \left[\sum_{n=1}^{N} (u_{ref}(n)) * \sum_{n=1}^{N} (u_{sig}(n)) \right]$$

It means, that the mean values of 3 different signals need to be calculated. The first is the mean value of analyzed signal multiplied by reference signal, the second one and the third one are mean values of analyzed signal and reference signal respectively. The described algorithm, real-time DC offset correction, does not require the memory space to archive sampled signals nor the changing of completed IC design.

Implementation

Method of the described real-time correction may be implemented by any DSP processor as easy as possible. In this experiment Analog Devices EZ-KIT Lite [3] has been used. This development kit contains DSP processor ADSP-2181 and 16-bit stereo audio codec AD1874 [1], as shown in Fig. 3.



Fig. 3: Functional diagram of Analog Devices EZ-KIT Lite development kit

The described method of DC component correction is appropriate when low-cost audio codecs are used in the design of lock-in amplifiers. Due to DSP processors it's easy to correct the created inaccuracy by the simple algorithm. High-resolution codecs can be used in this atypical application to improve the lock-in amplifier parameters.

Results

The described method of DC offset correction has been realized and verified. In order to determine the properties of designed instrument the signal generators HP33120A and Agilent 33240A were used. In order to preserve zero-phase shift between both input signal and reference signals, the generators were synchronized, as shown in fig. 4.



Fig. 4: Scheme of signal generators connection during the test

The results of tests are shown in following tables and figures. The digital output signal of lock-in amplifier was corrected by correction value calculated in real-time. Both of them are shown is the table 1 for the input signal range 0V - 2.8V and reference signal amplitude 2.668V.

	U _{оυт} [-]	U _{OUT-CRTD}	U _{OUT-CRTD}	$\Delta U_{OUT-CRTD}$
[V]	[-]	[-]	[V]	[mV]
0	9063	3	7,81E-05	0,078
0,1	12906	3846	0,1001	0,094
0,2	16778	7718	0,2009	0,865
0,3	20656	11596	0,3018	1,792
0,4	24515	15455	0,4022	2,224
0,5	28380	19320	0,5028	2,813
0,6	32242	23182	0,6033	3,323
0,7	36102	27042	0,7038	3,782
0,8	39962	30902	0,8042	4,240
0,9	43823	34763	0,9047	4,724
1	47360	38300	0,9968	-3,223
1,1	51197	42137	1,0966	-3,364
1,2	55030	45970	1,1964	-3,608

Table 1: Difference between corrected and uncorrected output digital value of designed lock-in amplifier - part 1

U _{SIG}	U _{OUT} [-]	U _{OUT-CRTD}	U _{OUT-CRTD}	$\Delta U_{\text{OUT-CRTD}}$
[V]	[-]	[-]	[V]	[mV]
1,3	58871	49811	1,2964	-3,644
1,4	62708	53648	1,3962	-3,784
1,5	66546	57486	1,4961	-3,898
1,6	70388	61328	1,5961	-3,908
1,7	74225	65165	1,6960	-4,048
1,8	78065	69005	1,7959	-4,110
1,9	81898	72838	1,8956	-4,355
2	85738	76678	1,9956	-4,417
2,1	89574	80514	2,0954	-4,583
2,2	93411	84351	2,1953	-4,723
2,3	97258	88198	2,2954	-4,603
2,4	101099	92039	2,3954	-4,639
2,5	104939	95879	2,4953	-4,701
2,6	109039	99979	2,6020	2,003
2,7	112632	103572	2,6955	-4,487

Table 1: Difference between corrected and uncorrected output digital value of designed lock-in amplifier - part 2

The fig. 5 shows the dependency of output digital signal of lock-in amplifier on amplitude of tested signal with and without the usage of correction algorithm.



Fig. 5: The output digital signal value vs. input tested signal amplitude

The designed lock-in amplifier measurement errors have been determined by following equations:

$$\varDelta_{\! u} = \frac{M}{100} * \delta_{FULL\,SCALE}$$

 $\delta_{FULL \,SCALE} = \frac{\Delta_u}{M} * 100$ $\delta_{FULL \,SCALE} = \frac{0,004724457}{2,695513086} * 100 = 0,175271139\%$

Error of measurement is 0,18% of full scale.

The described method of correction is able to improve the parameters of acoustic lock-in amplifier based on audio codecs. It also facilitate the application of the low-cost audio codecs in less typical applications.

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