A Beam Phase and Energy Measurement System Based on Direct RF Signal IQ Under-sampling Technology

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Abstract-A diagnostic system being designed to measure the beam phase and energy of the Drift Tube Linac (DTL) in the Proton Accelerator of China Spallation Neutron Source (CSNS) is described and the characterization of the prototype is presented. The signals received from Fast Current Transformers (FCTs) are Radio Frequency (RF) signals with the frequency up to 350 MHz and a dynamic range of -30 dBm to 3.5 dBm. The RF signals are converted to orthogonal streams directly with the In-phase and Quadrature-phase (IQ) under-sampling technique based on high-speed high-resolution A/D conversion. Thus a high quality sampling clock system is indispensable. Two different clock systems are implemented and tested for comparison. All Digital Signal Processing (DSP) algorithms are implemented in one single FPGA, meanwhile a Nios II embedded system is also integrated in it for data transfer through the Ethernet. This system achieves a phase resolution better than 0.07 degree over the input signal amplitude range of -41 dBm to 7 dBm.

Index Terms-CSNS, beam phase measurement, direct RF signal IQ under-sampling, high-speed high-resolution A/D conversion, Nios II embedded system

I. INTRODUCTION

The Time-of-Flight technique [1] is employed for beam energy measurement, which is implemented by measurement of the difference in phase of the beam signals from a pair of FCTs [2] with a known distance, so phase measurement is the kernel task for this system.

As for beam phase measurement, three basic methods are often employed: analog IQ demodulation, digital IQ demodulation and direct Intermediate Frequency (IF) signal IQ sampling. In the RF phasing system for the BEPCII LINAC, the analog IQ demodulation technique is used, and the system phase resolution is better than 0.2° over a dynamic range of 20 dB [3]; the phase measurement in the Spallation Neutron Source (SNS) low level RF control system is based on direct IF signal IQ under-sampling [4]. The basic method used in the beam phase and energy measurement for low Energy Demonstration Accelerator (LEDA) is the direct IF signal IQ sampling, and the system phase resolution is better than 0.12° over input amplitude range of -46 dBm to 10 dBm [5].

As for the analog IQ demodulation, it demands intricate analog electronics, and the phase errors are inevitable due to the mismatches of the analog IQ demodulation procedure [6]. The analog circuit of the digital IQ demodulation is relatively simpler, but the DSP algorithms are rather complicated [7]. To simplify the analog circuits design and the DSP algorithms, the direct RF signal IQ under-sampling technique is employed in this system which is implemented based on high-speed high-resolution A/D conversion. Thus a high quality sampling clock system is indispensable. Two different clock systems are implemented and tested for comparison.

II. SYSTEM ARCHITECTURE

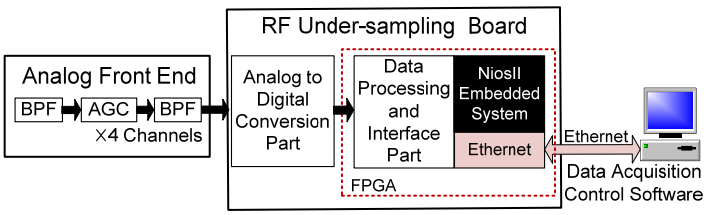


Fig. 1 Block diagram of the beam phase measurement system

This system consists of two hardware modules and a data acquisition software suite, as shown in Fig. 1. In the Analog Front End (AFE), the input RF signals with a dynamic range of around 48 dB are amplified by the

Automatic Gain Control (AGC) circuits to fit the Full Scale Range (FSR) of the ADCs on the RF Under-sampling Board (RFUB), and the Band Pass Filters (BPFs) are used as anti-aliasing filters for the under-sampling technique. The RFUB is composed of two parts -- the Analog to Digital Conversion Part and the Data Processing & Interface Part. All DSP algorithms are implemented in one single FPGA, meanwhile a Nios II embedded system is also integrated in it for data transfer through the Ethernet.

A. Analog to Digital Conversion Part

a) Considerations on the sampling clock frequency

The direct RF signal IQ under-sampling technique is used to convert the RF signals to digital I and Q streams for the phase and amplitude calculation. A careful choice of the sampling clock frequency is required to implement this method.
The RF signals from the AFE are sinusoidal signals, as in

$$y(t) = \sin(2\pi ft + \theta) \quad (1)$$

After sampling, the data sequence can be expressed as

$$Y(n) = \sin(2\pi fT_s n + \theta) \quad (2)$$

(T_s is the period of the sampling clock.)
The RF signal frequency f can be expressed as

$$f = K \times f_s \pm \Delta f \quad (\Delta f \le f_s / 2) \quad (3)$$

(f_s refers to the sampling frequency.)
With the equation (3), the equation (2) could be now expressed as

$$\begin{aligned} Y(n) &= \sin(2\pi fT_s n + \theta) \\ &= \sin\left[2\pi\left(K \times f_s \pm \Delta f\right)nT_s + \theta\right] \\ &= \sin\left(\pm 2\pi \Delta f n T_s + 2\pi K n + \theta\right) \\ &= \sin\left(\pm 2\pi \Delta f n T_s + \theta\right) \end{aligned} \quad (4)$$

Equation (4) indicates that the data sequence with frequency of Δf is obtained after sampling, whose phase value is identical to that of the RF signal. To meet the requirement of the IQ sampling, the following relation must be obeyed, as in

$$f_s = 4N \times \Delta f \quad (5)$$

Finally, the relation between the sampling rate and the RF signal frequency is as

$$f_s = \frac{4N}{4NK \pm 1} f \quad \left(f = Kf_s \pm \Delta f,\ \Delta f = \frac{f}{4NK \pm 1},\ N, K = 1, 2, 3...\right) \quad (6)$$

(f refers to RF Frequency; Δf refers to IF Frequency.)

b) Front-end circuits for A/D Converters (ADCs)

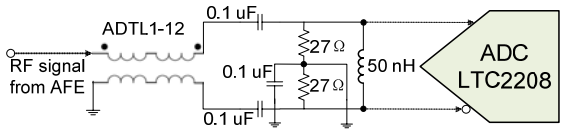


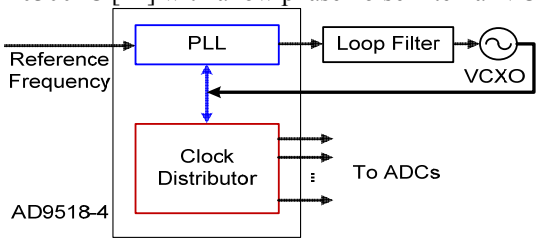
Fig. 2 Front-end configuration of the LTC2208 with balanced transmission line transformer

As for RF input signals, the front-end design of the ADC is a crucial element of the receiver design. The ADC front-end circuit of this system is shown in Fig. 2. This circuit is used to convert the single-ended signals to differential pairs, and to implement the impedance matching for input RF signal frequency, for which the values of the capacitors, inductors and resistors are carefully selected with the Agilent Advanced Design System (ADS) software. The balanced transmission line transformer ADTL1-12 used in this system is a wideband transformer with an insertion loss lower than 1 dB from 20 MHz to 1 GHz [8] .

c) Clock circuits design for ADCs

To achieve high resolution with the direct RF signal IQ under-sampling technique, high-speed high-resolution A/D conversion is required. As for the ADC, LTC2208-14 used in this system is a 130 Msps, 14-bit ADC with

an analog bandwidth up to 700MHz. The Signal to Noise and Distortion Ratio (SINAD) is about 71 dBFS at the frequency of 350 MHz [9]. Moreover, a high quality clock system is indispensable. Two different sampling clock systems are designed and tested for evaluation. Fig. 3 is the block diagram of the first clock system. A digitally controlled PLL chip (AD9518-4) with excellent jitter performance[10] and a high quality VCXO (VFVX120) [11] are used to generate the ADC sampling clock. Another precision clock conditioner LMK03001C [12] with a low phase noise internal VCO is used in the second clock system, as shown in Fig. 4.



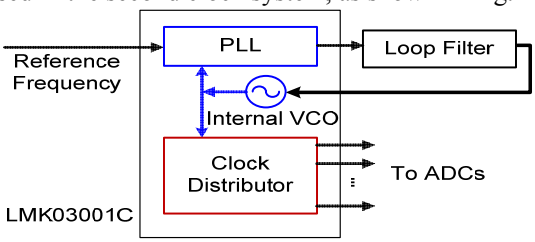


Fig. 3. Block diagram of the first clock system
Fig. 4. Block diagram of the second clock system

B. Data Processing & Interface Part

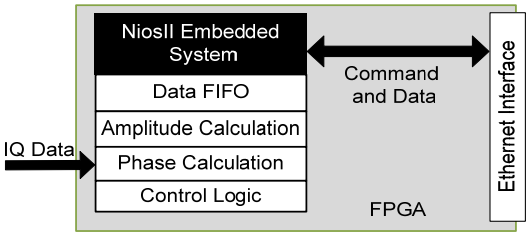
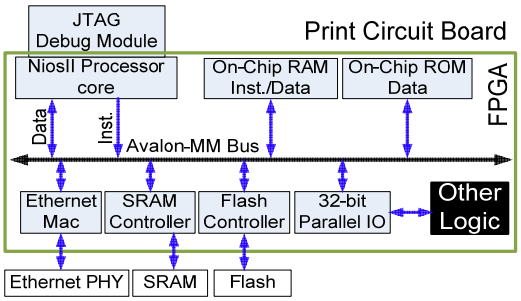


Fig. 5. Block diagram of the Data Processing and Interface Part

All data processing algorithms and interface part are implemented in one single FPGA, as shown in Fig. 5. The phase calculation block is implemented by the design of a non-linear look-up table (LUT), meanwhile the amplitudes are calculated by the algorithm designed with DSP Builder[13]. The Nios II Embedded system [14] is integrated to transfer data and receive the commands through the 100M Ethernet interface, rendering this system a stand-alone data acquisition and transfer system.



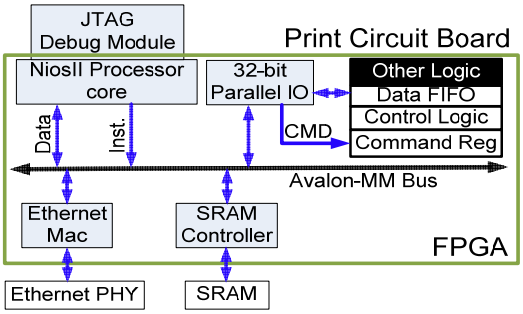


Fig. 6. Block diagram of the Nios II embedded system
Fig. 7. Block diagram of the data transfer interface controlled by Nios II Embedded System

The block diagram of the Nios II Embedded System is shown in Fig. 6. The Nios II Embedded System communicates with the remote PC through Ethernet interface and transfers the data and commands (CMD) through the 32-bit Parallel IO with other logic parts in the FPGA. The embedded software running on the Nios II system is stored in an external flash memory; the software is downloaded into an external SRAM memory (Cy7c1380c) [15] that functions as the system memory when the Nios II system is powered on.
Fig. 7 illustrates the data and command transfer process which is controlled by the Nios II embedded system. The external SRAM memory is used not only to store the embedded software, but also for data buffering. The Data FIFO functions as the data cache between the Nios II system and the data processing logic. The data from the Data FIFO is read out to the Nios II system and then written to the external SRAM in bulk mode, which will be further transferred to the remote computer through the 100M Ethernet interface. The intial test results indicate that a data transfer rate more than 1.3 MBps is achieved, which is faster than the requirement of the system update rate of about 32 KBps (corresponding to the real-time requirement on update rate of 2 kHz). The commands received by the Nios II Processor through the Ethernet interface are sent to the command registers,

and then decoded to activate different command signal lines to control the data acquisition and system configuration, as shown in Fig. 8.

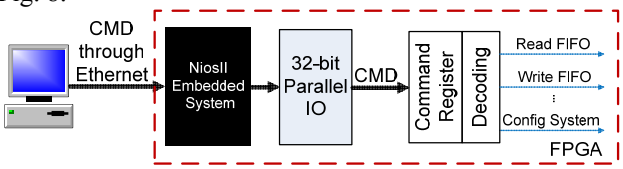


Fig. 8. Block diagram of the command transfer and decoding process

C. Design of The Software Suite

This software suite includes the Nios II embedded software based on the MicroC/OS-II and the GUI software running on the remote PC, which is responsible for the control of the data acquisition and results display. Socket programming is included in both parts to implement the communication through the Ethernet.

III. RESULTS OF INITIAL TESTING

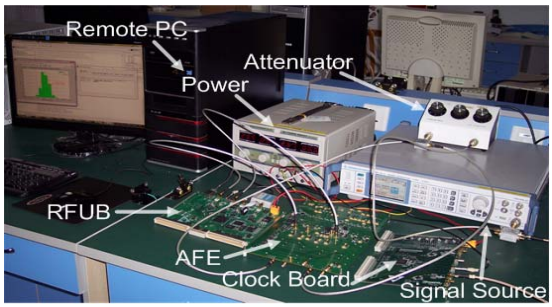


Fig. 9. System under test

As shown in Fig. 9, the input RF signals are manipulated in the AFE, and then transmitted to the RFUB for IQ under-sampling and data processing. A remote PC communicates trough the Ethernet with the Nios II embedded system which controls the data transfer. The tests are performed with the two clock systems mentioned above, with the results compared.

A. Results of the ADCs Test

The 352.2 MHz sine wave signal from the RF signal generator Rohde & Schwarz SMA100A is imported to the system, which is sampled by the ADC with 48.5793 MHz sampling rate that meets the relation shown in equation (6). Fig. 10 and Fig. 11 show the typical frequency spectrums of the ADC output signals (the input signals are both -11 dBm with a record length of 10240) respectively with the Blackman window adopted. The frequency spectrum of Fig. 10 is much cleaner nearby the frequency point of the input RF signal than that of Fig. 11; this corresponds to the different jitter performances of this two clock systems. Fig. 12 shows the Effective Number of Bit (ENOB) of the ADCs with different input amplitudes over the range of -41 dBm to 7 dBm. Test results indicate that the first clock system surpasses the second one in performance.

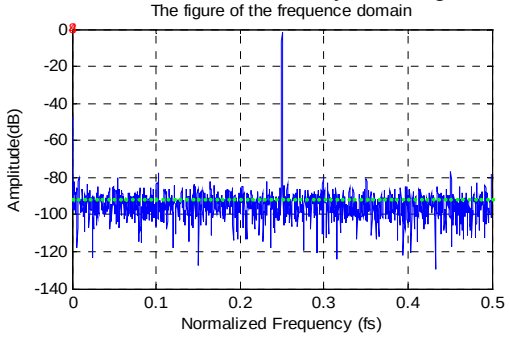


Fig. 10. Typical frequency spectrum of the ADC output signal with the first clock system

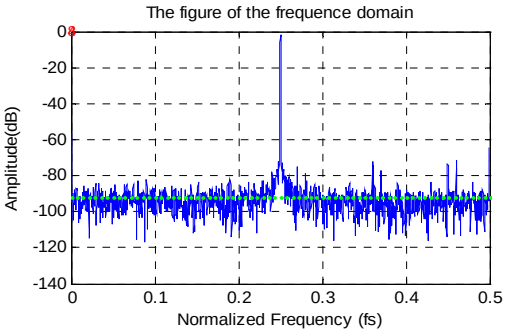


Fig. 11. Typical frequency spectrum of the ADC output signal with the second clock system

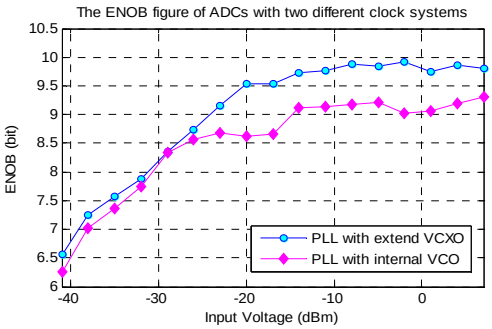


Fig. 12. The ENOB of ADCs with two different clock systems

B. Initial Results of Phase Measurement

Fig. 13 and Fig. 14 show the histogram of the phase result (input signals are both 0 dBm) with the update rate of around 12 MHz for the first and second clock system respectively.

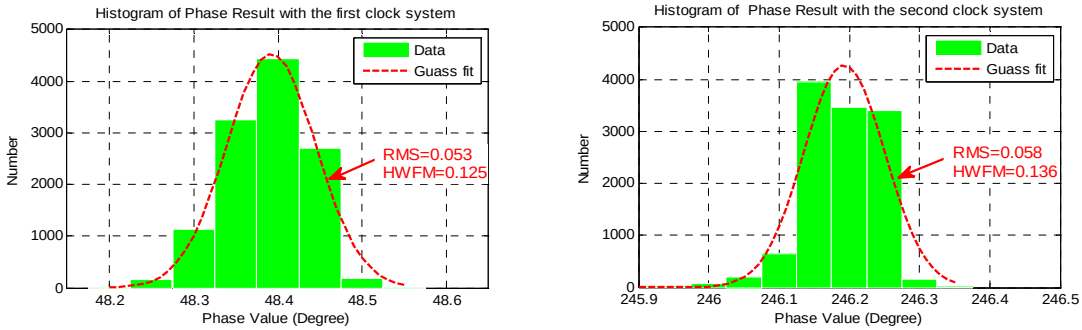


Fig. 13. Histogram of phase results with the first clock system
Fig. 14. Histogram of phase results with the second clock system

The phase resolution of the first clock system in the input amplitude range of -41 dBm to 7 dBm is shown in Fig. 15. The phase resolution is better than 0.25º, and enhanced to be better than 0.07º with data averaged per 32 points. Test results for the second clock system is shown in Fig. 16, which indicates that the phase resolution is better than 0.35º, and better than 0.12º with data averaged per 32 points. Phase measurement results also indicate that the first clock system performs better than the second one. This is probably due to the phase noise of the external VCXO used in the first clock system is lower than that of the VCO integrated in the PLL used in the second clock system.

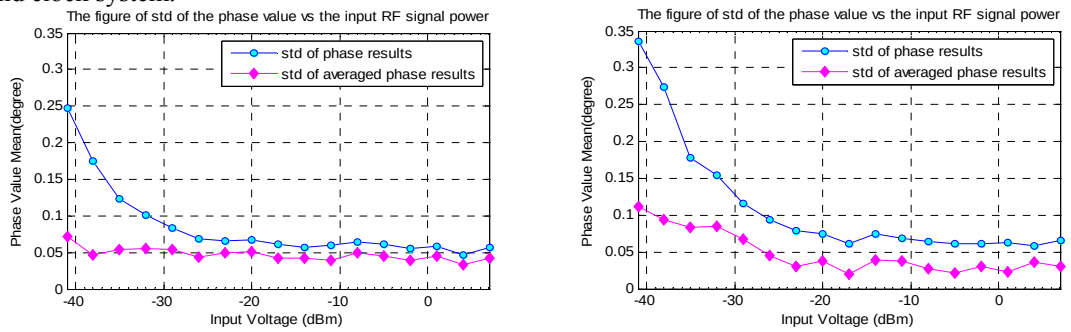


Fig. 15. Phase resolution result with the first clock system
Fig. 16. Phase resolution result with the second clock system

IV. CONCLUSION

The direct RF signal IQ under-sampling technique has been employed for the beam phase and energy measurement in this system. Two different clock systems have been designed and tested for comparison. This system has achieved a phase resolution better than 0.07º over the range of -41 dBm to 7 dBm with the first clock system. All the DSP algorithms and the data transfer interface are integrated within one single FPGA. Moreover,

it is a stand-alone data acquisition and transfer system by the implementation of the Ethernet interface and Nios II embedded system.

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