Novel Time-Interleaved Variable Centre-Frequency, Single-Bit A/D and D/A Sigma-Delta Modulator Topologies

Işıl Kalafat Kızılkaya, Mohammed Al-Janabi and Izzet Kale
Applied DSP and VLSI Research Group, University of Westminster, London, UK
Email: i.kalafat_kizilkaya@westminster.ac.uk, M.Al-Janabi@westminster.ac.uk, kalei@westminster.ac.uk

Abstract — This paper presents the design, modelling and analysis of novel multi-path time-interleaved analog and digital sigma-delta modulators that can operate at any arbitrary centre-frequency from DC to Nyquist. Dual- and quadruple-path fourth-order Butterworth, Chebyshev, inverse Chebyshev and elliptical based sigma-delta modulators are designed, which offer designers the flexibility of specifying the centre-frequency, pass-band/stop-band attenuation as well as the signal bandwidth. These topologies are compared in terms of their signal-to-noise ratios, hardware complexity, stability, tonality and sensitivity to non-idealities. In addition, this paper presents the mathematical modelling and evaluation of tones caused by the finite wordlengths of these digital multi-path sigma-delta modulators when excited by sinusoidal input signals.

I. Introduction

Sigma-Delta $(\Sigma - \Delta)$ modulators utilize oversampling and noise-shaping to accomplish high resolution in data converters, which result in simpler hardware when compared to their Nyquist-rate counterparts [1], [2]. However, discrete-time $\Sigma - \Delta$ modulators are mostly limited to narrowband signal applications due to their high oversampling requirements [1-5]. The Time-Interleaving (TI) technique overcomes this limitation by using M inter-connected $\Sigma - \Delta$ modulators working in parallel, where the processing speed of the modulator can be reduced by M times. A further advantage of the TI approach is that it offers an elegant means to increase the signal bandwidth for both A/D and D/A applications without the need to use faster or higher-order $\Sigma - \Delta$ modulators [3-5]. There are several behavioural- and circuit-level TI $\Sigma - \Delta$ modulator topologies reported in the open literature but to the best knowledge of the authors; all these topologies have concentrated on LowPass (LP) and mid-band resonator based $\Sigma - \Delta$ modulators [4-8].

In recent studies, analog multi-path TI variable-centre frequency $\Sigma - \Delta$ modulators were designed, analysed, evaluated and compared using ideal and non-ideal models [9], [10]. The first objective of this paper is to extend the principles proposed in [10] to the design of digital multi-path TI variable-centre frequency $\Sigma - \Delta$ modulators using the node-equation method. Furthermore, Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical based Noise Transfer Functions (NTFs) will be employed. These filter types allow designers to not only specify the centre frequency, but also the signal bandwidth therefore resulting in enhanced Signal-to-Noise Ratios (SNRs), Dynamic Ranges (DRs) and stability. The second objective will be to model, evaluate and compare the SNRs, DRs and stability thresholds of these multi-path $\Sigma - \Delta$ modulators with each other as well as providing a realistic means of evaluating their performance against their single-path counterparts.

One of the main challenges associated with the design of high-resolution single-bit quantizer digital $\Sigma - \Delta$ modulators is that they are highly tonal [11], [12]. However, it is a well-known phenomenon that single-bit $\Sigma - \Delta$ D/A converters require significantly less hardware when compared to their multi-bit counterparts, as the latter need extra Dynamic Element Matching (DEM) circuitry [2], [13]. Digital MASH $\Sigma - \Delta$ modulators, whose constituent $\Sigma - \Delta$ modulators employ single-bit quantizers, overcome this problem by reducing the quantization bits step-by-step in each block, therefore substantially alleviating the occurrence of spectral tones as well as ensuring modulator stability [14], [15]. The third objective of this study is to mathematically model the tonal behaviour caused by the finite wordlengths of digital variable centre-frequency single-bit based $\Sigma - \Delta$ modulators when excited by sinusoidal input signals.

II. Single Path Variable-Centre Frequency Σ-Δ Modulator Design

The first step of designing a SinglePath (SP) $\Sigma - \Delta$ modulator involves synthesising the NTF and mapping it to an appropriate topology [1], [2]. However, the mapping procedure requires a linearized model of the $\Sigma - \Delta$ modulator, which is conventionally achieved by approximating the non-linear quantizer to an additive white noise source. This approximation is adequate for preliminary design analysis. However, extensive simulations are required, as these utilize the actual single-bit quantizer, in order to verify the stability, tonality, SNR and DR of the designed $\Sigma - \Delta$ modulators [1], [2].

The generalized transfer function of an L^{th} -order BandStop (BS) NTF is given in (1) which can be obtained for a given design by specifying the filter type (i.e. Butterworth, Chebyshev etc), centre frequency, bandwidth as well as the attenuation parameters. Using the additive White noise model, this NTF can be then equated to the NTF of the chosen topology to enable the calculation of the coefficients of the corresponding loop-filter topology.

$$NTF(z) = \frac{\prod_{k=1}^{L} (1 - 2\alpha_k z^{-1} + z^{-2})}{1 + b_1 z^{-1} + \dots + b_{L-1} z^{-L+1} + z^{-L}}$$
(1)

In this paper, the 4th-order generalized NTF is mapped to the Output Feedback (OF) and Error Feedback (EF) topologies shown in Figure 1a and 1b. The cascaded integrators/resonators/delayers in the signal path of the OF topology may lead to input signal corruption which is not the case for the EF topology, whose Signal Transfer Function (STF) is one [16]. However, the EF topology is not practical for A/D applications, since the imperfections of the analog loop-filter are directly added to the input, therefore adversely affecting the output signal [1], [16]. For this reason, the EF topology is chosen for the D/A Σ - Δ modulator design whereas the OF topology is chosen for the A/D Σ - Δ modulator design.

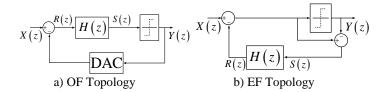


Figure 1: Block Diagrams of the Σ - Δ Modulator Topologies Deployed

Another design consideration involves determining an appropriate loop-filter topology. There are several studies in the literature that critically compare loop-filter topologies in terms of the resolution they provide as well as their sensitivity to non-idealities [1], [9]. In this paper, the Chain of delayed-Resonators with FeedForward and local Resonator FeedBack (CR-FF-RFB) topology will be used and is shown in Figure 2a. This topology has been selected, as it's less sensitive to non-idealities and generates smaller feedback coefficients when compared to the distributed feedback topologies [9]. Another advantage of this topology is that it employs delayed-resonators that can be easily realized using a single op-amp [17].

For the D/A topology, the Time Delay and Accumulate (TDA) topology, commonly known as direct form-1 IIR filter topology, shown in Figure 2b, is preferred as this topology uses smaller feedback and feedforward coefficients. Note that in this study, fixed-point representation is used where these implementations are likely to result in overflow due to the recursive nature of the IIR filters. Also instead of accumulators, delayers are used as the main building blocks to contain the internal signals, therefore preventing overflow and hence resulting in fewer internal data paths.

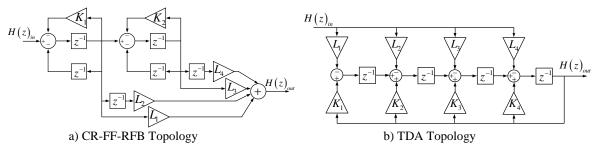


Figure 2: Chosen Loop-Filter Topologies

Table 1 summarizes the designed filter specifications and Table 2 shows their corresponding coefficients for both D/A and A/D based topologies.

Design Specs.	Butterworth	Chebyshev	Inv. Chebyshev	Elliptical
Centre-Frequency	0.21	0.21	0.21	0.21
Bandwidth	0.02	0.02	0.004	0.03
Passband Ripple	-	0.5 dB	-	0.5dB
Stopband Ripple	-	-	80 dB	80 dB

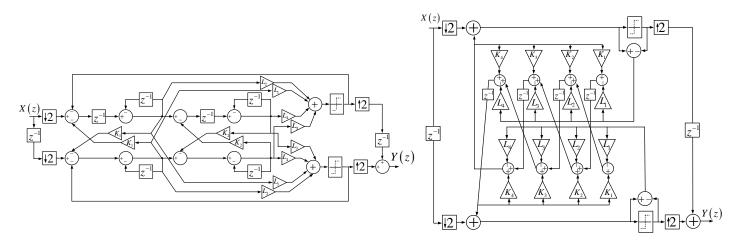
Table 1: Designed Filter Specifications

		K_1	K_2	K_3	K_4	L_1	L_2	L_3	L_4
Butterworth	A/D Topology	-0.4984	-0.4984	-	-	0.0442	-0.1628	-0.0136	~ 0
	D/A Topology	0.8372	-0.8713	2.0499	-0.9525	-0.1628	0.1253	-0.1984	0.0441
Chebyshev	A/D Topology	-0.4984	-0.4984	-	-	0.0302	-0.1114	-0.0090	~ 0
	D/A Topology	0.8886	-0.9110	2.1127	-0.9665	-0.1114	0.0858	-0.1357	0.0302
Inverse Chebyshev	A/D Topology	-0.5146	-0.4802	-	-	0.4630	-0.8250	-0.9804	0.0142
	D/A Topology	0.1750	-0.1214	0.2193	-0.5318	-0.8250	0.8734	-2.0278	0.4630
Elliptical	A/D Topology	-0.5011	-0.4980	-	-	0.0460	-0.1624	-0.0203	~ 0
	D/A Topology	0.8376	-0.8721	2.0440	-0.9533	-0.1624	0.1270	-0.2055	0.0459

Table 2: Feedback and Feedforward Coefficient

III. Multi-Path Variable-Centre Frequency $\Sigma - \Delta$ Modulator Design

TI Σ - Δ modulator design initially involves the construction of a working SP Σ - Δ modulator prototype, which can then be converted to its corresponding N-path TI counterpart using one of the techniques reported in [4], [5]. In [5], a polyphase decomposition methodology is proposed, but this requires complex mathematical analysis. On the other hand, the node equation method, originally proposed in [4] and further developed for the variable centre-frequency bandpass Σ - Δ modulators in [10], is easy to apply. It also uses fewer components when compared to the polyphase decomposition technique. The main idea of the node equation method is to write the node equations of the SP topology in the time-domain and individually convert these equations in a time-interleaved manner to construct a corresponding N-path topology. Figure 3 depicts the 2-Path TI topologies of the SP Σ - Δ modulator given in Figures 1, 2. Moreover, 4-Path topologies using this developed technique were designed, modelled and will be evaluated in Section V.



a) 2-Path CR-FF-RFB Topology

b) TDA Topology

Figure 3: Designed 2-Path TI Topologies

IV. Tonality

The quantization of a sinusoid creates tones, whose amplitudes and frequencies can be mathematically determined. This applies to variable-centre frequency $\Sigma - \Delta$ modulators when excited by sinusoidal inputs. Extra care must be taken especially in the case of digital $\Sigma - \Delta$ modulators as these tones are caused both by the quantizer and finite wordlengths. These tones can be modelled using the sawtooth quantization error model [18]. However, since the quantization error is highly input signal dependent, the actual power of these tones may become extremely difficult to predict.

Figure 4 depicts the additive white noise approximation of the quantizer [1]. The first step of the sawtooth quantization noise model is to use the additive noise model where the quantization error is defined as an input signal dependent sawtooth function. In Figure 5, the simulated quantization error of a sinusoid for a 1-bit quantizer is shown. As seen, the quantization error of a sinusoid is a sawtooth signal with a frequency of $2f_c$ multiplied by a sinusoidal signal with a frequency of f_c , where f_c is the input signal frequency.



a) Quantization block diagram

b) Linear model of the quantization

Figure 4: Additive White Noise Block Diagram

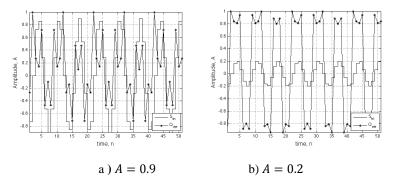


Figure 5: Quantization Error of a Sinosoid for a 1-bit Quantizer

Note that for an *m*-level quantizer, the frequency of the sawtooth signal will be $2mf_c$ as expressed in (2), where Q is the quantization step size and A is the input amplitude. Also, ε_1 and ε_2 are the input amplitude dependent errors that are assumed to have a white distribution. However, in this case they are assumed to be negligible and are approximated to zero.

$$Q_{err} = \left(\frac{A}{2} - \varepsilon_1\right) sawt(n) \frac{Q}{\left(\frac{A}{2} - \varepsilon_2\right)} cos(2\pi f_c n)$$
 (2)

$$sawt(n) = \frac{2}{\pi} \sum_{k=1}^{\infty} (-1)^{k+1} \frac{\sin(2\pi(2mf_c)n)}{k}$$
 (3)

$$Q_{err} = \frac{2Q}{\pi} \cos(2\pi f_c n) \sum_{k=1}^{\infty} (-1)^{k+1} \frac{\sin(2\pi (2mf_c)n)}{k}$$
 (4)

An ideal sawtooth wave function can be written as the sum of sinusoids with integer multiples of the fundamental frequency which is $2mf_c$ in this case (3). The process of calculating the quantization error signal is similar to double-sided AM modulation because the sawtooth signal is multiplied by a cosine (4). It is well known that, if a sinusoidal signal with a frequency of f_1 is AM-modulated by another sinusoid with a frequency of f_2 , the resulting tones will be at $(f_2 - f_1)$, f_2 , $(f_2 + f_1)$. Since $f_1 = 2mf_c$, $4mf_c$, $6mf_c$... and $f_2 = f_c$, the resulting tones will be at $[...(6m-1)f_c, (4m-1)f_c, (2m-1)f_c, (2m)f_c, (2m)f_c, (2m+1)f_c, (4m+1)f_c, (6m+1)f_c$...].

In order to explain this clearly, an example of the sawtooth quantization error model is given. It is assumed that a sinusoid with a normalized frequency of 0.15 (5) is applied to a 1-bit quantizer. This results in a quantization error of (6). For the ideal case, the quantization error is not input amplitude dependent and is represented by *A* as shown below.

$$S_{in} = A \cos(2\pi \ 0.15n) \tag{5}$$

$$Q_{err} = \frac{2Q}{\pi} \cos(2\pi \ 0.15n) \ \sum_{k=1}^{\infty} (-1)^{k+1} \frac{\sin(2\pi \ 0.3n)}{k}$$
 (4)

Figure 6a shows the spectrum of the sawtooth with a fundamental frequency of 0.3 and Figure 6b depicts its AM modulation by a cosine with a frequency of 0.15. It should be remembered that tones beyond 0.5 are folded back and added to the already existing tones within the range of [0, 0.5] as their frequency is mapped to $f_N - \lfloor f_N + 0.5 \rfloor$. The operator $\lfloor x \rfloor$ represents the largest integer less than or equal to $\lfloor x \rfloor$ and f_N is the normalized frequency of the signal.

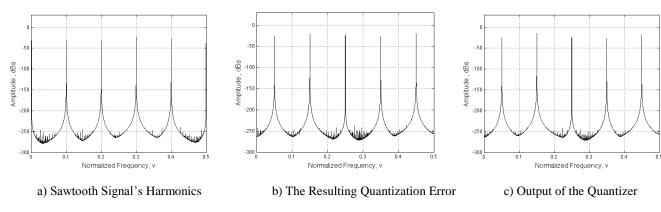


Figure 6: 1-bit Quantizer under Sinusoidal Excitation

Finally, Figure 6c shows the output of the quantizer that is equal to the sum of the quantization error shown in (6) and the input signal given in (5). The only difference between Figure 6b and 6c is the amplitude increase of the input frequency tone.

The sawtooth quantization error model can be summed up as follows:

- 1) The expected high tones in a Σ - Δ modulator resulting from the quantization of a sinusoid, not the limit cycle tones, can be calculated in terms of their frequency and amplitude. These tones are dependent on the input frequency, the number of the quantization levels and the quantization step size Q, but not the input amplitude.
- 2) These tones can be whitened by dithering, especially for multi-level quantizers due to their smaller Q resulting in lower amplitude tones when compared to the 1-bit quantizer. However, at some particular frequencies such as 0.25, 0.125, 0.375...etc dithering may not work sufficiently for all the tones. This is because harmonics of the sawtooth signal are mapped and added to each other at the same frequencies resulting in higher amplitude tones. On the other hand, variable centre frequency Σ-Δ modulators exhibit more but smaller amplitude tones that can be reduced sufficiently when dithering is employed. This makes the proposed topologies more attractive compared with their mid-band counterparts.
- 3) Input frequencies, whose values are irrational, result in a higher number of tones since the harmonics of the sawtooth signal are not folded back to the same frequencies. Therefore the resulting tones are expected to have lower amplitudes. On the other hand, it is apparent from (3) that the amplitude series of the sawtooth harmonics is divergent. Besides, irrational frequency tones are mapped close to each other and may not be sufficiently suppressed within the signal-band, thus resulting in significant SNR reduction. Figures 7, 8 illustrate this phenomenon where the outputs of the designed modulators with different centre-frequency inputs are determined.
- 4) The White noise approximation still applies as can easily be seen from the noise floor of the Figure 6. This noise floor is caused by ε_1 and ε_2 errors. Needless to say that in a Σ - Δ modulator, both the quantization noise and the tones will be accumulated and shaped.
- 5) As already explained, both the quantizer and the finite wordlengths of the D/A Σ - Δ modulators cause the sawtooth signal tones. Interestingly, the tones created by the finite wordlength effects are whitened during the accumulation process of the loop-filter since their amplitudes are very small for a 16-bit or higher wordlength quantization. However, for shorter wordlengths, they are not whitened sufficiently well and are subsequently processed by the 1-bit quantizer. Since these resulting tones' amplitudes are not input amplitude dependent, these finite wordlength based tones create extra tonality, which may result in Σ - Δ modulator instability. Moreover, using EF modulator topologies, as already explained, helps to diminish the finite wordlength based tones since the already whitened/accumulated feedback signal is extracted from the finite wordlength input sinusoid.

V. Simulations

The output spectrums of the SP and 2-Path TI Σ - Δ modulator topologies are presented in Figures 7, 8 for two different filter types and centre-frequencies where the effect of dithering on tonality is illustrated. A 16-bit input is used for the D/A simulations and internal limiters are employed to model the finite wordlengths of the Σ - Δ modulator.

In Figures 7a, 8a where dithering is not used, the modulated sawtooth harmonics can be easily seen. Figures 7b, 8b show that most of these tones are substantially reduced with modest amplitudes of dithering with the exception of the first five tones, which are quite hard to diminish. However, higher amplitude dithering will be needed to reduce the amplitude of these dominant tones, but at the cost of higher in-band noise quantization and consequently lower SNRs. Also in Figure 8 where an irrational input frequency is used, the output spectrum exhibits 3 high-amplitude tones as well as other small-amplitude harmonics in the signal band.

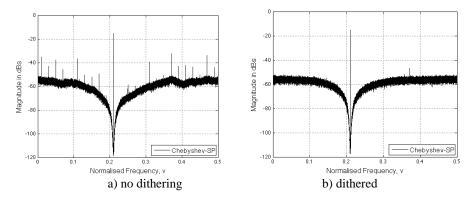


Figure 7: Output Spectrum for the D/A Topology; Chebyshev Filter, Centre-Frequency=0.21, BW=0.02, Stop Band Ripple=60 dB

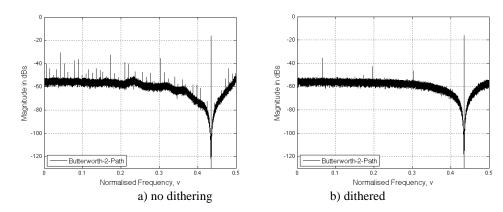
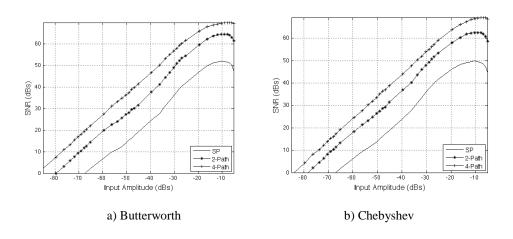


Figure 8: Output Spectrum for the A/D Topology; Butterworth Filter, Centre-Frequency= 0.43456, BW=0.015

The SNR curves of the SP, 2-path and 4-path Σ - Δ D/A modulators for an Oversampling Ratio (OSR) of 64 is shown in Figure 9 for the coefficients given in Section II. The effective OSR of the SP is 64, whilst it is 128 for the 2-path and 256 for the 4-path topologies. Extensive simulations for various centre frequencies and bandwidths demonstrate that the Inverse Chebyshev and Elliptical filters provide superior SNR values compared to their Butterworth and Chebyshev counterparts. This is attributed to the evenly distributed zeros and steeper transition bands of the former two which result in lower quantiztion noise power over the signal bandwidth. Furthermore, Inverse Chebyshev filters can be designed to have normalized bandwidths up to 0.001 (assumming Nyquist to be at 0.5) without causing the Σ - Δ modulator to become unstable.



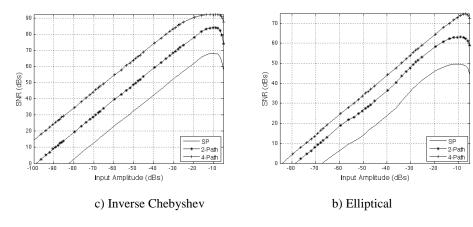


Figure 9: SNR Plots for the D/A Topology, OSR=64

The time-interleaving idea is built on the premise that perfect cancellation of the aliasing tones at the output summation block will be achieved [3], [4]. Channel mismatches within the structure prevent the cancellation of these aliasing tones resulting in an elevated noise floor and aliased limit cycle oscillations [3], [5]. These non-idealities are investigated for the analog TI Σ - Δ topologies in [9] and are also used in this paper to compare them with the effect of non-idealities in their digital counterparts. In the digital domain, the finite wordlengths cause loss of precision and create the tones that are detailed in Section IV. Compared with their analog counterparts, they inherit the stability and tonality properties of their corresponding SP topologies but do not suffer from mismatches.

VI. Conclusion

Novel variable centre frequency dual- and quadruple TI Σ - Δ modulators, which employ an assortment of filter types and topologies, were designed, modelled and analysed. The proposed TI Σ - Δ modulators are well suited for a wide range of A/D and D/A applications as they offer designers and practitioners the flexibility of defining the centre-frequency, bandwidth as well as the pass-band and stop-band parameters. The topology complexity, SNRs, stability and tonality of the aforementioned multi-path topologies were evaluated and compared with each other and against their single-path counterparts. The CR-FF-RFB was shown through analysis and detailed simulations to have greater robustness to coefficient mismatches. The direct form I topology was found to be more appropriate for digital implementation as it uses smaller coefficient wordlengths and fewer accumulators. Furthermore, the tones caused by the finite wordlengths of these digital multi-path Σ - Δ modulators, when excited by sinusoidal input signals, were mathematically modelled and verified through extensive simulations. The effects of these finite wordlengths on the spectral responses and resolution as well as a protorype implementation of these multi-path Σ - Δ modulators will be reported in a future publication.

REFERENCES

- [1] Norsworthy, S., Schreier, R., Temes, G., "Delta-Sigma Data Converters: Theory, Design and Simularion", "Willer-IEEE Press", 1997.
- [2] Candy, J., Temes, G., "Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation", "Willer-IEE Press", 1992.
- [3] A. Eshraghi and T. Fiez, "A comparative analysis of parallel delta- sigma ADC architectures," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 3, pp. 450 458, March 2004.
- [4] Kozak, M.; Kale, I.;, "Novel topologies for time-interleaved delta-sigma modulators," Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on, vol.47, no.7, pp.639-654, Jul 2000.
- [5] Khoini-Poorfard, R.; Lim, L.B.; Johns, D.A.; , "Time-interleaved oversampling A/D converters: theory and practice," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol.44, no.8, pp.634-645, Aug 1997.
- [6] Hwi-Ming Wang; Tai-Haur Kuo, "The design of high-order bandpass sigma-delta modulators using low-spread single-stage structure," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol.51, no.4, pp.202,208, April 2004.
- [7] S. Jantzi, K. Martin, and A. Sedra, "Quadrature bandpass delta; sigma; modulation for digital radio," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 12, pp. 1935 1950. Dec 1997.
- [8] M. Kwon, J. Lee, and G. Han, "A time-interleaved recursive loop band- pass delta-sigma modulator for a digital if cdma receiver," Circuits and Systems II: Express Briefs, IEEE Transactions on, vol. 52, no. 7, pp. 389 393, July 2005.
- [9] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, "Novel time-interleaved variable-center frequency sigma-delta modulators design, analysis and critical evaluation," accepted for publication, I2MTC 2013, USA, May 2013.
- [10] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, "Design and Evaluation of Time-Interleaved Variable Center-Frequency Sigma-Delta Modulators," accepted for publication, DSP 2013, Greece, July 2013.
- [11] I. Galton, "One-bit dithering in delta-sigma modulator-based D/A conversion," in Proc. IEEE Int. Symp, Circuits Syst., 1993, pp. 1310–1313.
- [12] K. Hosseini and M. P. Kennedy, "Maximum sequence length MASH digital delta-sigma modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2628–2638, Dec. 2007.
- [13] Chen, A.J.; Yong-Ping Xu, "Multibit Delta-Sigma Modulator With Noise-Shaping Dynamic Element Matching," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol.56, no.6, pp.1125,1133, June 2009.
- [14] Bornoosh, B.; Afzali-Kusha, A.; Dehghani, R.; Mehrara, M.; Atarodi, S.M.; Nourani, M., "Reduced complexity 1-bit high-order digital delta-sigma modulator for low-voltage fractional-N frequency synthesis applications," Circuits, Devices and Systems, IEE Proceedings , vol.152, no.5, pp.471,477, 7 Oct. 2005.
- [15] Fitzgibbon, B.; Kennedy, M.P.; Maloberti, F., "Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part II: Non-Constant Input," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol.59, no.9, pp.1980,1991, Sept. 2012.
- [16] Kiss, P.; Arias, J.; Li, D.; Boccuzzi, V.; , "Stable high-order delta-sigma digital-to-analog converters," Circuits and Systems 1: Regular Papers, IEEE Transactions on , vol.51, no.1, pp. 200- 205, Jan. 2004.
- [17] T. Salo, S. Lindfors, and K. Halonen, "A double-sampling sc-resonator for low voltage bandpass delta; sigma;-modulators," *Circuits and Sys- tems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 49, no. 12, pp. 737 747, Dec 2002.
- [18] Abuelma'atti, M.T., "Spectrum of a nonlinearly quantised equal-amplitude dual-tone signal," Circuits, Devices and Systems, IEE Proceedings , vol.148, no.1, pp.11,18, Feb 2001.