

# Real, Reactive and Apparent Power Computing Using FPGA and PWM Intermediary Conversion

Catalin Damian, Cristian Zet, Cristian Fosalau, Mihai Cretu

"Gh. Asachi" Technical University of Iasi, Faculty of Electrical Engineering, Bd. D. Mangeron, 53, 700050, Iasi, Romania, phone +40232278680, Fax +40232237627, cdamian@ee.tuiasi.ro, czet@ee.tuiasi.ro, cfosalau@ee.tuiasi.ro, mcretu@ee.tuiasi.ro

**Abstract-** In the paper, an instrument for simultaneous measurement of active, reactive and apparent power is presented. Its functionality is based on a PWM intermediary conversion multichannel analog to digital converter (ADC). The instrument is implemented on an Altera's Flex10k70 Field Programmable Gate Array (FPGA) device for single phase. It fits roughly 60% of logic cells without any resource sharing algorithm. All the operations are executed in a parallel mode, providing a very short execution time.

## I. Introduction

Electric power monitoring is a very important task in many industrial applications. An efficient power management is the key to industrial progress. Traditional power measurements have been performed in both time and frequency domains. The time domain approach is the most efficient and the most accurate when root mean square (rms) and real power as well as their dependent quantities are computed. This is because the starting point for all digital methods are the voltage and current waveforms concurrently sampled at uniform intervals over one or more cycles [1]. The frequency domain can offer better results for distortion and harmonic influences but suffers when it deals with non-stationary signals.

The power analyser described here is based on a method that differs from those implemented in electrodynamic, electrostatic, thermal and Hall effect wattmeters. These are classical instruments in which the power value results from physical phenomena or are computed by software algorithms using specialized signal processors. In FPGA, the multiplication involves discrete numbers without introducing instrumental errors but those specific to signal processing (truncation, rounding, sampling, etc.) Additionally, the digital method opens up possibilities of performing very fast power measurements, which may be valuable in power control applications, and also of measuring nonsinusoidal waveforms with greater accuracy [2].

FPGAs are very powerful, relatively inexpensive and adaptable devices because their configuration is specified by an abstract description language. The presented instrument offers better performances compared with software solutions with lower clock speeds (digital signal processor or microprocessor).

## II. Theory of calculation

This section describes the theory of real, reactive and apparent power, rms and power factor calculation. Definitions of various types of powers are found in the IEEE Standard Dictionary of Electrical and Electronics Terms [IEEE Std. 100-88] [3].

If  $v_t$  and  $i_t$  are periodic signals with period  $T$ , then the real power  $P$  is given as follows:

$$P = \frac{1}{T} \int_0^T i_t v_t dt \quad (1)$$

Reactive power is defined as a "quantity measured by a perfect watt-hour meter which carries the current of a single-phase circuit and a voltage equal in magnitude to the voltage across the single-phase but in quadrature therewith" [4]. At each frequency over its range, the voltage  $v_t$  leads the voltage in quadrature  $v_{t-90^\circ}$  by  $90^\circ$ . If  $v_{t-90^\circ}$  and  $i_t$  are periodic signals with period  $T$ , then the reactive power  $Q$  is given by [1]:

$$Q = \frac{1}{T} \int_0^T i_t v_{t-90^\circ} dt \quad (2)$$

In this paper, the reactive power will be computed from the power triangle:

$$Q = \sqrt{S^2 - P^2} \quad (3)$$

where  $S$  is the apparent power, being calculated as product between the rms voltage  $V$  and the rms current  $I$ . The above equation (3) is true only for sinusoidal waveforms.

$$S = V_{rms} I_{rms} \quad (4)$$

The rms value is a basic measurement for an ac signal magnitude. It can be defined under practical or mathematical aspects. Practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Mathematically, the rms value of a continuous signal  $V(t)$  is defined as:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2(t) dt} \quad (5)$$

For time sampling signals, the rms calculation presumes squaring the signal, taking the average, and obtaining the square root:

$$V_{rms} = \sqrt{\frac{1}{N} \sum_{i=1}^N V^2(i)} \quad (6)$$

The power factor (PF) registers the ratio between the real power and the apparent power consumed by a load:

$$PF = \frac{P}{S} \quad (7)$$

### III. The proposed block diagram

The block diagram of the developed instrument is presented in Figure 1. The voltage and current signals are obtained from a voltage transducer ( $VT$ ) and a current transducer ( $CT$ ) respectively. First of all, a signal conditioning is performed in order to scale the measuring signal supplied to the analog to digital converter (ADC) input. The unknown signal is compared with a triangular signal in the analogue section of the ADC. The triangular signal is generated by the triangle wave generator ( $TWG$ ) synchronized with FPGA clock via the frequency divider ( $FD$ ).

The information is carried on by a PWM (Pulse Width Modulated) signal between the analogical and the digital parts of the ADC [5]. In the digital part of the ADC ( $D-ADC1$  and  $D-ADC2$ ), two counters are used to get the information from the PWM signal and to translate it into 12 bit digital format. The simultaneous sampling multi-channel ADC has been presented in [5].

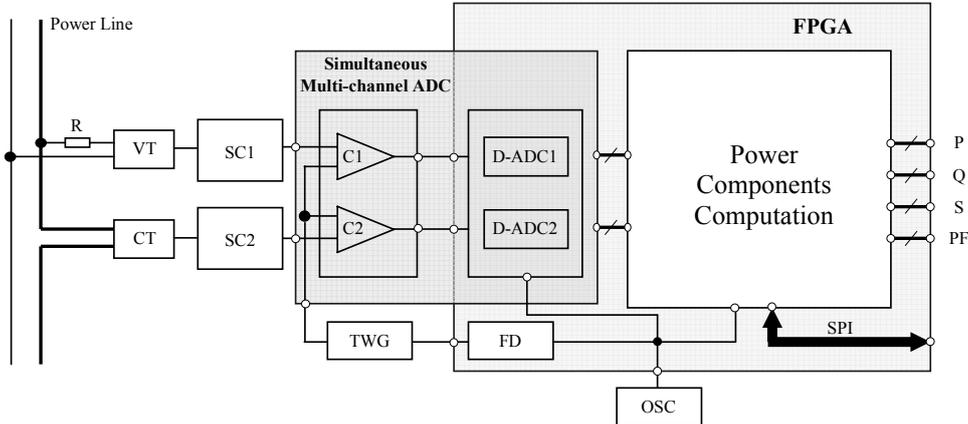


Figure 1. Block diagram of the power analyser

Using a 25 MHz clock frequency and 12 bits of resolution, the sampling frequency results to be around 6 KHz. In this case, the ADC will compute 120 samples per period for 50Hz power line frequency. The samples are processed into the FPGA synchronized with the clock signal. A critical part of the measurement process is the timing between the sampling frequency and the start of conversion. In this case, the problems are no longer important, while they are synchronized. The sampling frequency ( $F_s$ ) is obtained with a divider from the system clock:

$$F_s = \frac{F_{OSC}}{2^n} \quad (7)$$

where  $F_{OSC}$  is the oscillating frequency of the FPGA (the counting clock) and  $n$  is the ADC resolution

in bits. A greater sampling frequency can be obtained decreasing the ADC's resolution.

#### IV. Power parameters computing instrument

The arithmetical blocks are implemented into a Flex10k70 device using Quartus II development software. Figure 2 presents the architecture of this implementation. Digital components of the ADC are not presented here. Each voltage and current sample is sent to a Finite Impulse Response filter (FIR) for a primary filtration. The filter coefficients, generated using a FIR Compiler Software (MATLAB, GNU Octave or Scilab), are read from a ROM memory using a serial interface. This makes the filter programmable regarding the frequency response and its type.

After the filtering stage, a binary code conversion is made (BCC). The ADC samples values are in offset binary code and for digital processing the data must be in two's complement format. To convert the format, the MSB of the each sample is inverted.

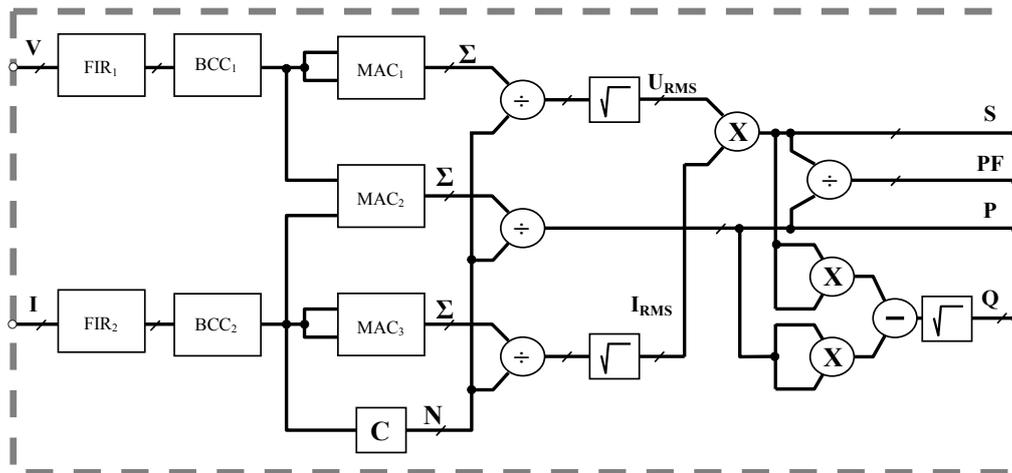


Figure 2. Computing algorithm implemented in FPGA

Next, the samples are multiplied and accumulated by a MAC (multiply and accumulate) block. These operations are synchronized with the other operations, on the basis of two general signals: *clock* and *clear* (Figure 3). The counter (C) detects the signal period generating the “*clear*” signal and the number of samples per period (*N*). Before clearing the MAC registers, the values are loaded into dividing blocks registers.

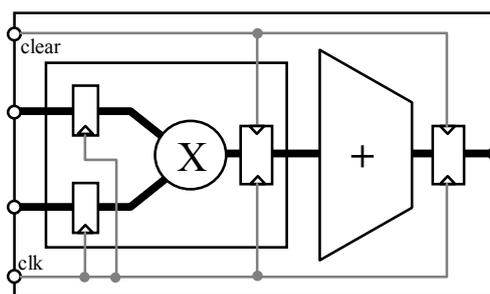


Figure 3. Multiply and Accumulate Diagram

$MAC_1$  computes the  $\Sigma V^2$ ,  $MAC_2$  is computing the  $\Sigma VI$  and  $MAC_3$  is computing the  $\Sigma I^2$ . An MAC entity for a 12 bits data occupies around 250 logical cells. This represents about 6,5% from the total number of Flex10k70 logic cells.

The square root operation is implemented in VHDL (VHSIC hardware description language) using a non-restoring algorithm [6]. This block occupies less than 100 logic cells from a total number of 3800. The computing time is around 1  $\mu$ s.

Using other digital blocks (multiplying, dividing, subtracting) power factor, real, reactive and apparent powers are computed. These values can be directly displayed or used for controlling a process and/or sent to another device via a Serial Peripheral Interface Bus (SPI).

## V. Conclusions

A general purpose instrument for measuring the power parameters has been presented. Its functionality is based on an ADC using PWM intermediary conversion [5]. This instrument can be used for power monitoring and can be easily interconnected with any other instrument or software tool that uses a digital interface. It provides real time information about power components like real power, reactive power, apparent power and power factor. The main advantages are related to small occupied area, fast computation and to the possibility of expanding to three phase systems.

## References

- [1] Weon-Ki Yoon, Michael J. Devaney, "Reactive power measurement using the Wavelet transform", *IEEE Transactions on Instrumentation and Measurement*, vol. 49, pp. 246-252, 2000.
- [2] Raymond S. Turgel, "Digital wattmeter using a sampling method", *IEEE Transactions on Instrumentation and Measurement*, vol. IM-23, pp. 337-341, 1974.
- [3] P. S. Filipski, Y. Baghzouz, and M. D. Cox, "Discussion of power definitions contained in the IEEE dictionary", *IEEE Transactions Power Delivery*, vol. 49, pp. 1237-1244, 1994.
- [4] B. Djokic, P. Bosnjakovic, M. Begovic, "New method for reactive power and energy measurement", *IEEE Transactions on Instrumentation and Measurement*, vol. 41, pp. 280-285, 1992.
- [5] C. Zet, C. Damian, C. Foşalău, "New type ADC using PWM intermediary conversion", *Proceedings of the 12<sup>th</sup> TC4 International Workshop on ADC Modelling and Testing*, Iasi, Romania, pp. 113-117, 2007.
- [6] K. Piromsopa, C. Apornetewan, P. Chongsatitvatana, "An FPGA implementation of a fixed-point square root operation", *International Symposium on Communications and Information Technologies*, pp. 587-589, 2001.
- [7] A. Sarkar, S. Sengupta, "A low-cost fault-tolerant real, reactive, and apparent power measurement technique using microprocessor", *IEEE Transactions on Instrumentation and Measurement*, vol. 56, pp. 2672-2680, 2007.
- [8] Weon-Ki Yoon, Michael J. Devaney, "Power measurement using the wavelet transform", *IEEE Transactions on Instrumentation and Measurement*, vol. 47, pp. 1205-1210, 1998.
- [9] Daniel Sharon, "Power factor definitions and power transfer quality in nonsinusoidal situations", *IEEE Transactions on Instrumentation and Measurement*, vol. 45, pp. 728-733, 1996.