ADC DYNAMIC RANGE IMPROVEMENT FOR WIDEBAND HF RECEIVERS

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INTRODUCTION

The development of 14 bit monolithic Analogue to Digital Converters (ADC's) capable of sampling at 80 MHz [1] has revived interest in digitising the entire 3-30 MHz High Frequency (HF) radio spectrum for use in wideband HF receivers [2,3,4]. This enables the ADC to be placed close to the antenna so removing the need for analogue mixing as well as offering a multi-channel reception capability, using multiple digital synthesisers and direct conversion I, Q mixing to baseband, as indicated in Figure 1.

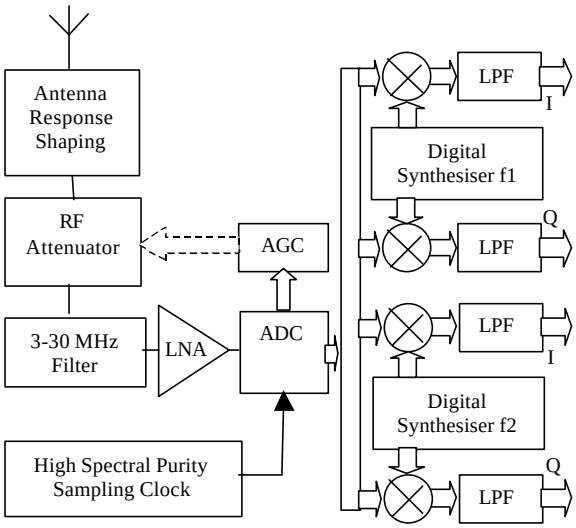

Figure 1 Multi-Channel Wideband HF Receiver

A number of performance benefits also accrue, as traditionally difficult receiver design aspects such as image rejection and internally generated spurs associated with analogue mixing are no longer an issue. Also only one fixed frequency local oscillator signal with high spectral purity is required, ie the ADC sampling clock. The ADC does, however, have to accommodate the very large number of signals present in the HF spectrum over a large dynamic range without introducing distortion.

While the use of 14 bit monolithic ADC's sampling at 80 MHz has demonstrated such a capability for communications purposes [3, 4], the dynamic range is still somewhat short of that necessary to achieve the highest performance, particularly in receivers for HF radar without the use of pre-selection filters [2].

An improvement in effective dynamic range is possible in principle by operating a number of such ADC'c in parallel and summing the outputs digitally. This however only gives a 3 dB (1/2 bit) improvement for each doubling of the number of devices used, which soon becomes impractical, even with low cost monolithic devices.

This paper examines an alternative approach using a two-stage RF feedforward technique as a possible means of achieving the desired improvement in dynamic range.

DYNAMIC RANGE REQUIREMENTS

The demands of an ADC capable of accommodating the entire HF spectrum without distortion are quite formidable. The converter must be capable of accommodating many high level signals simultaneously, particularly those from high power HF broadcast station carriers. These can each produce in the region of –30 dBm at the receiver input, even with spectral shaping in the antenna matching network to offset the variation of external noise with frequency. The total signal power can easily be 20 dB higher at –10 dBm, and a further 10 dB allowance for occasional peaks leads to a maximum in the region of 0 dBm. Automatic Gain Control (AGC) in the form of a variable attenuator ahead of the ADC is also generally necessary to accommodate an inevitable variation with propagation conditions [3, 4].

The noise floor of the converter must be low enough to provide a noise figure for the receiver of better than 12 dB for communications purposes and closer to 6 dB at the higher frequencies for HF radar [5]. This translates to a spurious free dynamic range (SFDR) requirement of 127 dB in a 3 kHz resolution bandwidth, and a signal to noise spectral density ratio of at least 162 dBc/Hz, increasing to 168 dBc/Hz for HF radar.

The maximum rms signal to rms noise ratio in the half sampling rate S/N (fs/2), for a sinusoidal signal just filling the range of an ideal n bit converter, can be shown to be given by:

$$S/N\ (fs/2) = 6.02\ n + 1.76\ dB \quad \ldots\ldots (1)$$

Provided the quantising noise is spread uniformly from dc to the half sampling frequency, the signal to noise spectral density in dBc/Hz is given, for fs in Hz, by:

$$S/N\ (1Hz) = 6.02\ n + 10\ \mathrm{Log}\ (fs/2) + 1.76\ dBc/Hz \quad \ldots (2)$$

The equivalent number of bits resolution necessary to achieve a given signal to noise spectral density is then:

$$n = [S/N\ (1Hz) - 10\ Log\ (fs/2) - 1.76] / 6.02\ \text{Bits} \quad \ldots\ldots (3)$$

Thus for an ADC sampling at 80 MHz, an S/N(1Hz) of 162 dBc/Hz requires a resolution equivalent to an ideal quantisation of 14 Bits, and 15 bits for HF radar.

The signal to noise ratio achieved by an ADC in practice is inevitably somewhat less than that indicated by the number of bits generated, due, in a Nyquist sampling ADC, to differential non-linearity (DNL) and the influence of sampling clock aperture jitter in the input sample and hold. The signal to noise ratio for the 14 bit monolithic ADC described in [1], for example, is quoted as typically 74.5 dB for a tone at 1 dB below full scale. Taken to be in the half sample rate, sampling at 80 MHz, this corresponds to an effective resolution of 12.25 bits.

The low noise amplifier (LNA) shown preceding the ADC in Figure 1 is used to re-position the dynamic range of the ADC to achieve the necessary noise figure, requiring an additional allowance for the noise figure of the amplifier. The linearity of this amplifier, and of the analogue input stages of the ADC, including any sample and hold, must be sufficient to prevent the generation of intermodulation noise from the many signals in the HF spectrum, and of discrete intermodulation products from high level broadcast station carriers. For the highest performance a third order intercept point in excess of 40 dBm and a second order intercept point in excess of 80 dBm, referred to the LNA input, is required [5].

Intermodulation products generated by the converters in [1] for example, are typically around 100 dB below overload for two tones each at 7 dB below overload, indicating a third order intercept point of + 39.5 dBm, and second order of + 86 dBm, for 0 dBm overload. This suggests that the analogue input stage, including the sample and hold, has just sufficient linearity. Unlike a purely analogue circuit, the intermodulation products associated with the quantiser do not reduce with tone level to give a constant intercept point, but remain approximately constant in level. Fortunately, in a wideband HF receiver, however, the input signal appears sufficiently noise-like to provide spectral spreading of the intermodulation product or spur energy [3]. Band-limited noise can, at the expense of some loss in dynamic range, be added to the converter outside of the HF passband to assist in this spectral spreading.

The dynamic range achieved by Nyquist sampling monolithic converters such as those described in [1] is therefore still somewhat short of that ideally required. An improvement of around 25 dB, to give at least an equivalent ideal 16 bit performance, appears necessary for the highest performance receivers, to allow for the input amplifier noise figure and to reduce the amount of AGC required. This is likely to require a design target of 17-18 bits to allow for implementation losses, as well as some improvement in sample and hold aperture jitter.

FEEDFORWARD ARCHITECTURE

The two-stage RF feedforward arrangement shown in Figure 2 offers a possible means of achieving the desired improvement in dynamic range, and linearity, by operating two ADC's in cascade. The technique has been applied to extending the dynamic range and linearity of two third order continuous time bandpass sigma-delta ADC's for use in narrowband HF radar receivers [6]. It is similar in principle to the two-pass technique frequently adopted in Nyquist sampled monolithic ADC's, except the error signal is returned to continuous time form, by means of a low pass filter, before application to the second stage, obviating the need for a sample and hold at the input.

In the first stage, the analogue input signal is applied to a short cable delay line and high linearity low noise buffer amplifier having a combined transfer function k_1. The input signal is also applied via buffer amplifier k_A to an A-D converter ADC(A), contributing quantising noise n_A. The output from the digital to analogue converter (DAC) is then subtracted from the analogue input signal by combining with the output from the amplifier k_1. The amplifier k_D represents the transfer function of the DAC.

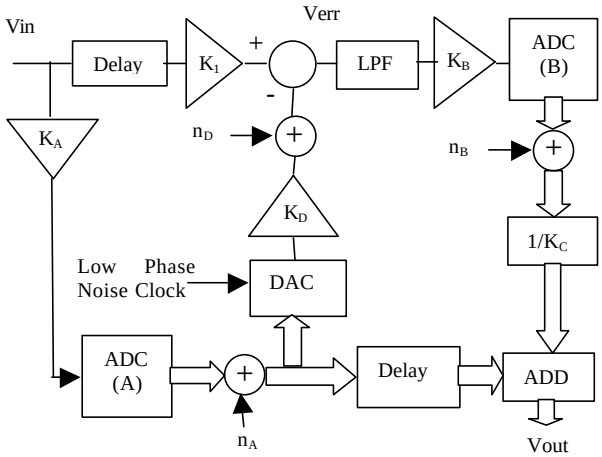

Figure 2 Two-Stage RF Feedforward Architecture

Provided the signal path through amplifier k_A, ADC(A) and the DAC matches that through the cable delay line and amplifier k_1, to within better that about 0.25 dB in magnitude and 2 degrees in phase, the error signal Verr resulting from the subtraction will be at least 25 dB below the input range of ADC(A). Verr can then be amplified by up to 25 dB, after low pass filtering, and applied to a second A-D Converter ADC(B) having the same input signal range as ADC(A). Verr is given by:

$$Verr = Vin\ [k_1 - k_A\ k_D] - n_A\ k_D - n_D \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

The output from ADC(B), contributing quantising noise n_B, is then attenuated by a convenient binary factor factor k_C close to 25 dB (eg 16), and added to the output from ADC(A) delayed by a digital delay as indicated.

Assuming initially that this delay compensates for the delay introduced by the low pass filter, the output from the adder, Vout, is given by:

$$Vout = Vin\ k_A + n_A + Verr\ [\ k_B / k_C\ ] + n_B / k_C \ldots\ldots\ldots (5)$$

Using (4) and re-arranging gives:

$$Vout = Vin\ k_1\ k_B / k_C + Vin\ k_A\ [1 - k_D\ k_B / k_C\ ]$$

$$+ n_A\ [1 - k_D\ k_B / k_C\ ] - n_D\ k_B / k_C + n_B / k_C \ldots (6)$$

.

If $k_B / k_C = 1 / k_D$ then

$$Vout = Vin\ k_1 / k_D - n_D / k_D + n_B / k_C \ldots\ldots\ldots\ldots\ldots (7)$$

Thus provided the second stage feedforward paths are matched to give sufficient suppression of the quantising noise n_A from the first ADC, the principal noise contributions will be from the DAC (ie n_D / k_D) and the second ADC, with the latter reduced by k_C (ie n_B / k_C). Vout will equal Vin with a small scaling factor (k_1 / k_D), which represents the transfer function of the DAC relative to the amplifier k_1.

CALIBRATION

Matching of the signal paths in each stage of the arrangement of Figure 2 requires a calibration procedure and the inclusion of equalisers as indicated in Figure 3

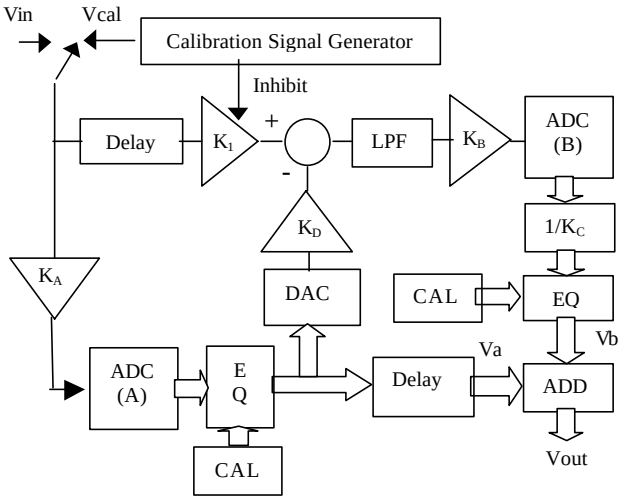

Figure 3 Calibration Signal Generator and Equalisers

The equaliser in the first stage must compensate for response differences in the two signal paths from the analogue input port to the low pass filter input sufficiently to limit the maximum signal that is applied to ADC(B). Provided the ADC response is sufficiently flat over the required signal passband the equaliser can be reduced to a simple adjustment of gain and delay.

The equaliser in the second stage must compensate for response differences in the two signal paths from the output of ADC(A) to the output of the adder sufficiently to suppress the quantising noise from ADC(A). As this includes the response of the low pass filter, as well as general gain and delay differences, an N tap FIR equaliser becomes necessary.

The calibration is performed by switching the converter input to a locally generated calibration signal producing a comb of tones spaced across the converter passband. The peak envelope level of this signal however needs to be at least 25 dB below ADC(A) overload to prevent overloading ADC(B), requiring at least 1k point FFT analysis to provide adequate signal to noise ratio during measurement.

During calibration of the second stage, performed first, the amplifier k_1 is disabled to provide isolation from the input. The calibration signal, quantised by ADC(A), is then passed equally through both paths of the second stage including the DAC. The signal at each input to the adder, Va and Vb in Figure 3, with the equaliser set to unity, is then captured for FFT analysis, from which the relative amplitude and phase response is computed, and from this the equaliser tap coefficients.

Calibration of the second stage requires that

$$[1 - k_D\ k_{LPF}\ k_B\ k_{EB} / k_C\ ] = 0$$

where k_{LPF} is the response of the low pass filter relative to the digital delay at the input to the adder, giving the desired equaliser response k_{EB} as

$$k_{EB} = k_C / (k_{LPF}\ k_B\ k_D) \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

From Figure 3

$Va = Vcal\ k_A$ and $Vb = - Vcal\ k_A\ k_D\ k_{LPF}\ k_B / k_C$, giving

$$Va / (-Vb) = k_C / (k_{LPF}\ k_B\ k_D) = k_{EB} \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Calibration of the first stage requires that the error signal Verr is minimised, ie $[k_1 - k_A\ k_{EA}\ k_D] = 0$, giving the required equaliser response k_{EA} as:

$$k_{EA} = k_1 / (k_A\ k_D) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

The calibration is performed with amplifier k_1 enabled, the second stage equalised and the first stage equaliser set to unity. Then from equation 7 and ignoring the noise contributions:

$Vout = Vin\ k_1 / k_D = Vcal\ k_1 / k_D$, giving

$$Vout / Va = k_1 / (k_A\ k_D) = k_{EA} \ldots\ldots\ldots\ldots\ldots\ldots (11)$$

Thus the equaliser response is again obtained by FFT analysis of captured data, in this case of Va and Vout, from which the required gain and delay adjustment can be computed.

CRITICAL PERFORMANCE ASPECTS

The most critical parts of the arrangement of Figure 3 affecting the overall performance are the analogue signal path through the calibration switching, cable delay and buffer amplifier k_1, to the subtractor and the DAC.

The calibration switching can be arranged to avoid the use of any relays or distorting the signal path by adding the cal signal to the input port as a current and inhibiting the low noise input amplifier preceding the converter, as well as the buffer amplifier k_1. The calibration does not depend on the absolute accuracy of the calibration signal.

The non-linearity and noise contributions from the cable delay are unlikely to have any appreciable effect provided the amount of delay required is not excessive.

Established RF amplifier techniques can be applied to the design of the low noise input amplifier and buffer amplifier k_1 to achieve sufficient linearity and noise performance. Moreover, the use of a differential current output for the buffer amplifier k_1, summed in the input impedance of the low pass filter, with a differential current output DAC, reduces the output voltage swing to that of the error signal. A current output also facilitates implementation of an inhibit function and reverse isolation. The latter is necessary in the case of the input amplifier to prevent radiation from the antenna during calibration and in the buffer amplifier k_1 to prevent the DAC output returning to ADC(A).

The quantising noise, spurs, and contributions from non-linearity in the first ADC are suppressed in the second stage, once calibrated, while those from the second ADC are reduced by the binary division factor kc. When calibrated therefore, the overall signal to noise performance is critically dependent on the performance available from the DAC as the noise n_D is not suppressed. To achieve the desired improvement in overall dynamic range and linearity, the performance of the DAC must therefore exceed that of the component ADC's by around 25 dB, ie achieve a resolution equivalent to an ideal 16 –17 bits at 80 MHz sample rate.

DAC PERFORMANCE

A conventional multi-level DAC will depart from the ideal due to systematic level errors (differential non-linearity) and also from code dependent irregularities during transitions between levels. If applied to the low pass filter without a sample and hold the latter will produce additional spurs if generating CW tones. For the noise-like HF signal however spurs should be spread and only contribute to an increased in the noise floor. A sample and hold at the DAC output however may still suffer from breakthrough during large transitions between samples, which will be integrated by the filter, again contributing additional noise.

The most linear form of DAC for generating continuous time signals is a single bit converter supplied with a 1-bit sigma-delta signal. The converter then simply consists of a high speed switch. Generation of the sigma-delta signal however requires an oversampling factor of around 100, leading to a sampling rate of at least 3 GHz to cover the 3-30 MHz HF band. While initially appearing impractical, transistors with f_T's in excess of 100 GHz are now available with which such a high speed switch might be implemented in monolithic form.

Differential non-linearity should not be an issue with just two levels in a 1-bit DAC. Performance is however limited by any pattern dependence of pulse width, if using a return to zero data signal, or by the imbalance between positive and negative transitions if using non-return to zero (NRZ) data. The latter will generate the equivalent of a series of narrow pulses aligned with one polarity of transition in the NRZ data stream, equivalent to differentiation and rectification of the sigma-delta signal, producing an associated noise floor with an approximately uniform spectrum.

A single bit DAC used in [6], driven by NRZ data at a sample rate of 10 MHz, achieved a floor of around –150 dBc/Hz, equivalent to a maximum signal to noise ratio of 83 dB in 5 MHz. Transition times were in the region of 1-2 ns with matching adjusted manually without great difficulty. Assuming that the same proportional degree of matching could be maintained in a single bit DAC operating at 3 GHz, a noise floor in the region of -175 dBc/Hz might be achieved (ie $-83 - 10 \log (1.5 \times 10^9)$), offering some margin over that required.

Phase noise is also an important issue in the DAC. Jitter on the DAC clock and in the DAC switch will be transferred directly to the DAC output, producing phase noise on the signals being passed by the sigma-delta signal, depending on their frequency. A jitter amplitude of 0.1 ps for example, ie 1% of say a 10 ps transition time, equates to a phase noise –167 dBc/Hz on a single 30 MHz signal [3]. The summation of this noise from many signals at different frequencies, for a mean total signal level 10 dB below overload, suggests a noise floor of around –177 dBc/Hz, again giving some margin. Phase noise on the 3 GHz clock source can of course be filtered before application to the DAC, noting also that a given amplitude of time jitter at 3 GHz will produce 40 dB less phase modulation at 30 MHz than at 3 GHz.

IMPLEMENTATION

The sigma-delta signal necessary to supply the single bit DAC could be produced either by a sigma delta modulator supplied from a 14 bit monolithic ADC sampling at 80 MHz, or by a single bit sigma-delta ADC directly. Sampling at 3 GHz should provide a resolution for the modulator or ADC of 12-13 bits across 30 MHz, ie similar to that realised in practice by a 14 bit Nyquist sampled ADC. The modulator approach would however

require a stage of interpolation to increase the 80 MHz sample rate from the ADC to 14 bits at 3 GHz. Also the 14 bit ADC may introduce a number of sample periods of delay at 80 MHz, requiring a long cable delay line.

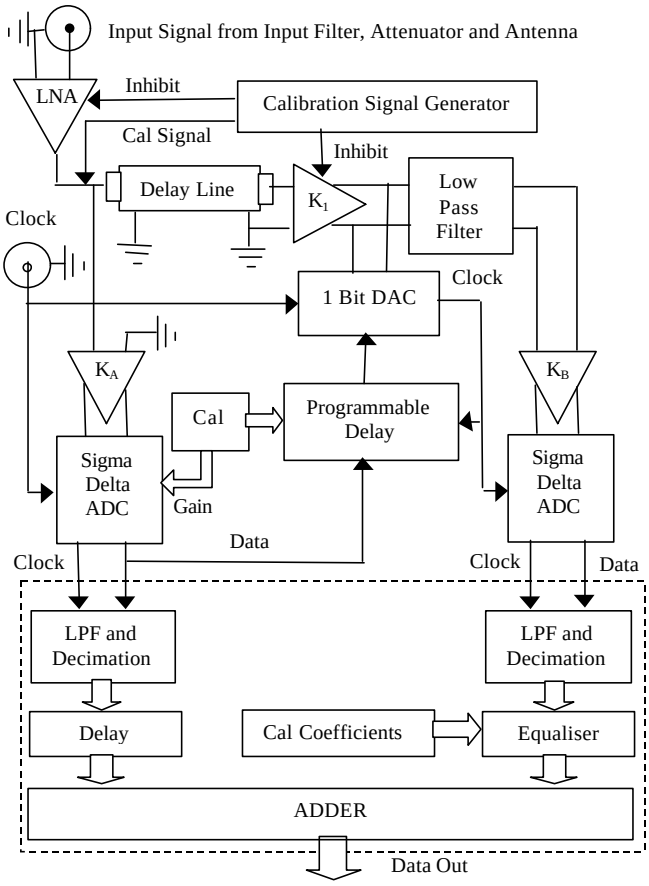

Figure 4 Possible Converter Arrangement using Sigma-Delta ADC's

Figure 4 shows a possible arrangement using two sigma-delta ADC's. Since the DAC output within a sigma-delta converter feedback loop is constrained to follow the analogue input signal, the delay through each ADC should be only one or two 3 GHz sample periods, thus limiting the length of analogue delay cable required. This also allows a programmable delay in increments of 333ps to be inserted in the output from the first ADC, allowing +/- 1.8 degrees incremental phase adjustment on a 30 MHz signal. Gain control in the first loop is achieved by adjusting the current in the DAC of the sigma-delta ADC. The simple 1 bit data and clock interfaces to the digital signal processing section, shown dotted in Figure 4, permits isolation of the sensitive analogue section using optical coupling if required.

In the digital signal processing section, the output from the first stage ADC is low pass filtered and decimated to 80 MSamples/s for delay and addition with a similar output from the second ADC. Equalisation for the second stage uses an N tap FIR filter, and includes the scaling factor k_C. The value of N will depend on the response correction required for the low pass filter.

CONCLUSIONS

The paper has examined a two stage RF feedforward technique as a possible means of achieving an improvement in dynamic range over that currently achievable using 14 bit monolithic ADCs, sampling at 80 MHz, for use in wideband HF receivers. The approach would however require the development of a baseband sigma-delta ADC sampling at 3 GHz, to provide 12-13 bit equivalent resolution up to 30 MHz, an associated digital low pass filter and decimation stage and a low jitter high speed current switch 1-bit DAC.

Improvements in the capability of Nyquist sampling monolithic ADC's operating at 80 – 100 MHz to give the required dynamic range with reduced aperture jitter would be a preferred solution, offering low cost and avoiding the need for calibration. However the two-stage approach examined offers potentially higher capability as the performance is ultimately determined by that of an inherently linear, low spurious, single bit DAC, no sample and hold is required at the input and no sharp analogue anti-aliasing filters are necessary.

ACKNOWLEDGEMENT

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